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K. Sivasankaran
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Multigate Transistors for High Frequency Applications

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Preface

The world is celebrating the 75 Years of Transistors in the 2022–2023 academic year. The transistor is one of the most important inventions in history which changed the world. We would like to present this book to the readers as a part of this celebration. The three American Physicists John Bardeen, Walter Brattain, and William Shockley demonstrated their invention (a tiny Ge Chip with metal point contacts) at Bell Labs, USA, on December 16, 1947. That was the beginning, a significant improvement of the transistors had happened during the last 75 years. The prediction of the great philosopher Gordon Moore played an important role in this development. He said that transistor density in integrated circuits will double every 18 months. The world is moving toward reducing the size of transistors to accommodate more in number, lesser power consumption, smaller delay, better performance, and reliability. However, the downscaling of conventional planar metal-oxide-semiconductor field-effect transistors (MOSFETs) is creating many problems such as the increase in leakage currents and short channel effects (SCEs). Most of the problems due to short channel effects and leakage currents in MOSFETs can be solved by improving the controllability of the gate. Researchers introduced multigate FETs instead of single-gate MOSFET to have better controllability of the channel. The multigate FETs provide better performance in terms of higher on current (I_{on}), lower off current (I_{off}), and SCE suppression capability. With the evolution of these multigate transistors with shorter gate lengths, the high-frequency capabilities of transistors reached the GHz regime and the radio frequency (RF) circuit applications have been steadily growing.

There exist several textbooks on multigate transistors, some of these books focus mainly on the physics and technology of multigate FETs, and a few titles are available with circuit applications of multigate FETs. However, to our knowledge, no book contains a detailed study on the high-frequency applications of these devices. This book contains seven chapters.

Chapter 1 shows the impact of scaling followed by a detailed report on the roadmap of semiconductor devices for RF applications. Also, the evolution of the multigate transistors is presented.

In Chap. 2, a detailed theory on Figures of Merit (FoM) of RF transistors and RF stability is presented followed by the design challenges of FET devices for RF applications.

Chapter 3 presents the stability factor modeling of DG MOSFETs. The gate and drain bias dependency on RF stability performance is discussed. The impact of gate spacer length and silicon body thickness on RF stability performance of DG MOSFETs is discussed, and finally, the bias and geometry optimized DG MOSFETs are presented.

RF stability performance and the impact of process variation on RF stability performance of DG Tunnel FET are presented in Chap. 4. A non-quasi static model is presented to extract the device's small-signal parameters. The optimized device parameters are listed after the detailed process variation study to operate DG Tunnel FET for RF applications.

Chapter 5 presents an RF stability model for FinFET followed by a detailed study on bias and geometry dependency on RF stability of FinFET. The study illustrates the geometrical parameters like fin thickness, fin height, and spacer length and gate and drain biases with gate metal work function that has an impact on RF stability performance. Finally, the optimized device parameters are presented.

In Chap. 6, the bias and geometry optimization of SNWT are discussed. The RF stability modeling is presented followed by a detailed study on the effect of silicon radius and gate alignment on the RF stability performance of silicon nanowire transistor.

Chapter 7 provides an insight into the RF stability performance of SELBOX ITJLFET, and also the impact of bias and geometrical parameters on the RF stability of the device is presented.

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Contents

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Dr. Partha Sharathi Mallick working as a Professor Higher Academic Grade in the School of Electrical Engineering at Vellore Institute of Technology (VIT), Vellore, India. He served the same institution as the Dean of School of Electrical Engineering from 2011 to 2015. Dr. Mallick and his research teams developed "Online Lab in Microelectronics" "Monte Carlo Simulator for Compound Semiconductors" "Nanostructured MIM Capacitor" and "Low-cost Electric Fencers". IET Springer, and Scitech published his 4 books and book chapters; Dr. Mallick has published 128 research papers in reputed international journals till December 2021. Dr. Mallick organized the Science, Engineering, and Technology conferences at University of Cambridge in 2018 and at Indiana University—Purdue University (IUPUI), USA in 2019. Dr. Mallick organized IEEE International Conference on Advances in Electrical Engineering at VIT jointly with KTH, Sweden in 2014. He visited 38 top universities of the world for different academic assignments, invited lectures, collaborations, and organizing conferences. His research interest includes CNT Applications, Compound semiconductors, reliability of electronic devices and circuits.

Chapter 1
Introduction

Abstract Device scaling is one of the major challenges which was extensively studied by researchers and engineers in the last five decades. There exists a trade-off between performance and area of the chip. The introduction of multigate transistor mitigates major scaling issues and improves device performance on chip. This chapter provides a detailed insight on impact of scaling, evolution of multigate transistor, and roadmap for semiconductor devices for RF applications.

Keywords Scaling · More than Moore · Multigate transistors · Radio frequency

1.1 Impact of Scaling

Complementary metal oxide semiconductor (CMOS) technology is leading microelectronics industry. The size of the transistor has been scaled down continuously for many technology generations, resulting in consistent improvement in both device density and performance. Specifically, there is a constant drive to make transistors that occupy less space which is responsible for smaller feature size and increase in clock speed that implies the assumption of the continuation of Moore's law stated by Moore (1965), which states that the transistor density on integrated circuits doubles in every 18 months. The continuous scaling of CMOS devices provides the advantage of larger device density and high performance which are the primary factors for high-speed integrated circuits. The ability to improve performance while decreasing power consumption has made CMOS the dominant technology for very large-scale integration (VLSI) circuits. Scaling down of conventional CMOS transistors face barriers due to the fundamental physics limitation often cited such as (1) quantum–mechanical tunneling of carriers through the thin gate oxide; (2) quantum–mechanical tunneling of carriers from source to drain, and from drain to the body of the metal oxide semiconductor field effect transistor (MOSFET); (3) control of the density and location of dopant atoms in the MOSFET channel and source/drain region to provide a high on–off current ratio, and (4) the finite subthreshold slope. These fundamental limits have led to the end of technological progress in the semiconductor industry.

Figure 1.1 shows the technology introduction year, the transistor count for microprocessors, and Moore's law. In 1971, the transistor count on a chip is 2300 with

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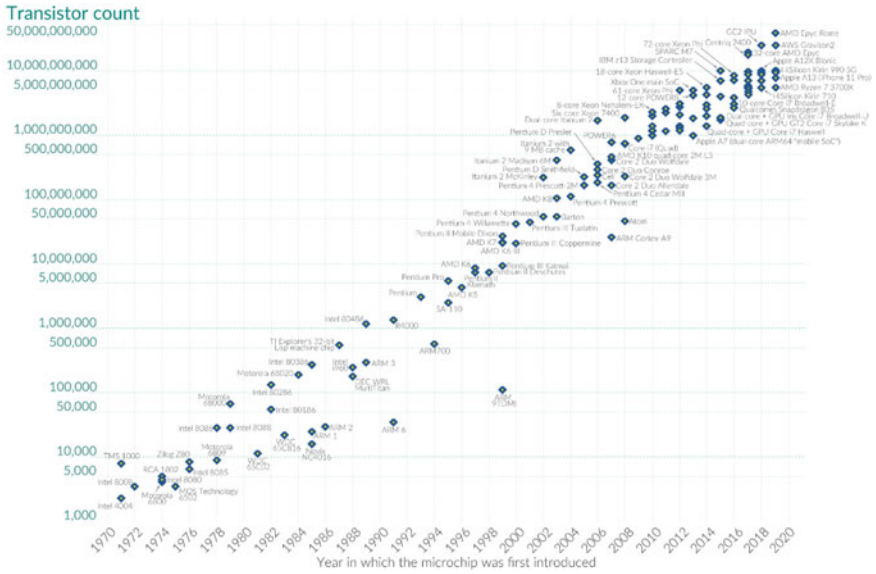

Fig. 1.1 Transistor count of microprocessor versus year of introduction

the rapid technology scaling over the last five decades. In 2020, the transistor count reached 50,000,000,000. To meet Moore's law requirement, it requires innovations in device engineering such as multigate structures, graded doped channels, compound material for source and drain regions, metal gate, and high-k dielectric for gate oxide.

1.2 Heterogeneous Integration of Digital and Non-Digital Functionalities

In a digital integrated circuit, the CMOS transistor is the basic component to build the logic device, memory, and other components. In many applications, the integrated circuits will have non-digital functionalities and they should operate in a user environment. A more complex system that uses integrated circuit (IC), passive components, etc., is assembled on a printed circuit board (PCB). The paradigm shifts from PCB to the integrated chip are because of trends in processing technology and the design of CMOS and non-digital technologies.

Figure 1.2 depicts the need for heterogeneous integration of digital and non-digital functionalities in a product. As per Moore's law, scaling results in the miniaturization of devices which leads to performance improvement as per the International Technology Roadmap for Semiconductor. The application of new structure novel materials, and processing steps to improve the performance of the transistors. In the functional diversification of devices shown in Fig. 1.2, non-digital functionalities also

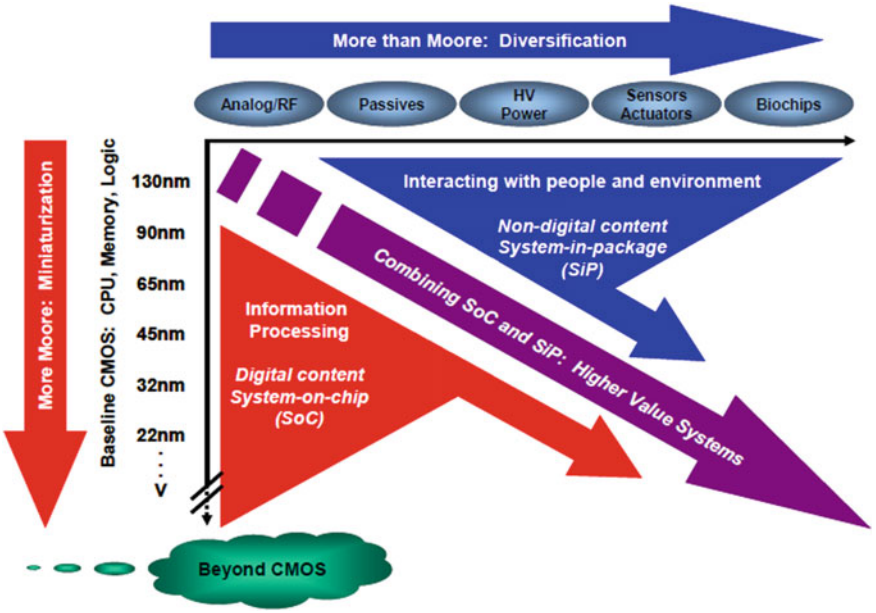

Fig. 1.2 Miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore")

can contribute to the miniaturization of electronic systems even though they are not scaled according to Moore's law which predicts the development of digital functionality. Because of added functionality, this trend is designated as "More-than-Moore" (MtM).

Functional diversification is regarded as a complement of digital signal and data processing in a product. This includes the interaction with the outside world through appropriate transduction (sensors and actuators) and the subsystem for powering the product. These functions may imply analog and mixed-signal processing, the incorporation of passive components, high-voltage components, micro-mechanical devices, sensors and actuators, and microfluidic devices enabling biological functionalities. It should be emphasized that "More-than-Moore" technologies do not constitute an alternative or even competitor to the digital trend as described by Moore's law. It is the heterogeneous integration of digital and non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security, and entertainment. Whereas "More Moore" may be viewed as the brain of an intelligent compact system, "More-than-Moore" refers to its capabilities to interact with the outside world and the users.

1.3 Evolution of Multigate Transistors

A multigate MOSFET refers to a metal oxide semiconductor field-effect transistor (MOSFET) that has more than one gate in a single device. The multiple gates may be controlled by a single-gate electrode, wherein the multiple-gate surfaces act electrically as a single gate, or by independent gate electrodes. The most widely used multigate devices are the Fin field-effect transistor (FinFET) and the gate-all-around field-effect transistor (GAAFET), which are non-planar transistors, or 3D transistors. The evolution of multigate transistor is shown in Fig. 1.3.

In the late 1980s, double-gate Si MOSFETs were initially demonstrated on SOI substrate. The purpose of the back gate is to tune the threshold voltage V_T of the front-gate transistor Lim et al. (1983). Meanwhile, multigate transistors, like double-gate FinFET and GAA MOSFETs were demonstrated also on SOI substrate, as the insertion of buried oxide could eliminate the substrate leakage and simplify the process steps for fin-to-fin isolation. In 1999, Huang et al. (1999) demonstrated the first FinFET with a gate length L_G of sub-50 nm and a fin width of 15−30 nm. Later some of the leading research groups and foundries like IBM, STMicroelectronics, Intel, TSMC, and Samsung demonstrated the technology of their multigate gate field effect transistor with excellent control of short channel effects and decent transfer characteristics.

1.4 Roadmap of Semiconductor Devices for High-Frequency Applications

Radiofrequency (RF) devices receive and transmit signals from 3 kHz to 300 GHz, covering a variety of wireless applications Joseph et al. (2005). Broadcasting at radio frequencies has been an established technique for almost a century. Cellular phones have been used for decades. New generations of cellular phones (5G) have just been available. Moreover, wireless local area network (Wi-Fi) is gaining popularity for laptop, tablet, and smartphone users, since Wi-Fi can provide access to the Internet via an access point (hotspot). Campus-wide Wi-Fi and city-wide Wi-Fi are providing added facilities to these users. Other applications of RF include global positioning systems (GPS), phased array RF systems, radio frequency identification devices (RFIDs), and smart handheld devices Zhao (2006). Since wireless communication enables voice, data, image, and video to be transferred anywhere instantaneously, the impact of RF devices on people's daily lives has become significant.

In the first five decades of the twentieth century, vacuum tubes were used as active devices in RF applications. These vacuum tubes were unreliable, bulky, and consume large power. Since the invention of transistors, researchers have put a lot of effort to operate transistors for high-frequency applications and replacing vacuum tubes. The first bipolar transistor using germanium (Ge) was developed in 1958–1959 and operated at 1 GHz and above. The dominance of Ge transistors in RF applications

declined as silicon-based transistors received more attention in semiconductor electronics. Silicon bipolar junction transistors (BJTs) began their operation in 1963, and in 1970, almost all RF transistors were silicon BJTs Cooke (1971). Silicon BJTs and gallium arsenide (GaAs) metal semiconductor field effect transistors (MESFETs) were the only two RF transistor types used in the 1970s and early 1980s. In the 1980s, rapid improvements in GaAs MESFET were found, whereas the progress in Si BJT took place gradually. Silicon BJTs were used for frequencies below 4 GHz, whereas in the frequency range between 4 and 18 GHz, the GaAs MESFET was the better choice.

Table 1.1 shows the major milestones in the development of the RF transistor Schwierz et al. (2007), Božani´c (2019). It is evident that till the early 1970s, Ge and GaAs-based transistors were used as microwave transistors. In late 1970, the first microwave transistor with high electron mobility was patented. Since the inception of high electron mobility transistors (HEMTs) in the 1980s, the device was studied by many researchers to find its potential for RF applications. After the 1990s, RF transistor research on Si MOSFETs devices occurred, but the fact that Si MOSFETs are relatively slower. The Si MOS technology-led Si MOSFET has gradually become a candidate for RF applications. In 2001, a large variety of different competing devices and technologies were available, including Si CMOS, Si BJT, SiGe HBT, GaAs MESFET, GaAs HEMT, GaAs HBT, InP HEMT, InP HBT, and wide bandgap FETs. In 2007, an InP HEMT transistor with a $f_{\max}$ of more than 1 THz with a gate length of 35 nm was demonstrated by Deal et al. (2011) and Mei et al. (2015). In 2013, a 25 nm node was reported, with a maximum oscillation frequency ($f_{\max}$) of 1.5 THz. In 2016, 130 nm HBT technology was demonstrated by Urteaga et al. (2016), showing a $f_{\max}$ of 1.15 THz. Each of the different transistor types has certain advantages and disadvantages in terms of maturity, cost, and performance. In the mass consumer markets, all technologies can compete, but Si-based technologies have a clear cost advantage.

Figure 1.4 shows the reported cut-off frequency (f_t) and maximum oscillation frequency ($f_{\max}$) values of Si MOSFETs versus time and demonstrates the progress in the MOSFET frequency performance (Schwierz and Liou 2007). Beyond 2005, f_t and $f_{\max}$ cross 300 GHz. It is also interesting to see that, after a long period of stagnation between the 1990s and 2000, the $f_{\max}$ performance of Si MOSFETs shows a considerable increase beyond the 2000s. Many devices were studied beyond 2000, and Table 1.2 shows recorded f_t, $f_{\max}$ values of Si-MOSFET during mid-2007. It shows that for the scaled device there is a steep increase in f_t as well as $f_{\max}$. Furthermore, by 2020, a unity gain cut-off frequency of 790 GHz and the maximum oscillation frequency of 1.11 THz are to be achieved at a gate length level of 11 nm.

Table 1.1 Major milestones in the development of RF transistors

Year	Milestone
1947	First BJT presented
1948	Basic heterojunction bipolar transistor (HBT) patent
1958	First microwave transistors (Ge BJT)
1965	GaAs MESFET introduced
1973	First transistor with $f_{\max} = 100$ GHz
1978	Basic high electron mobility transistor (HEMT) patent
1980	HEMT introduced
1982	First successful experiment on III-V HBTs
1985	pHEMT introduced
1987	First SiGe HBT
1988	First mm HEMT
1995	First III-V FET with $f_{\max} > 500$ GHz
1996	First Si-MOSFET with $f_T > 200$ GHz
1999	III-V HBT with $f_{\max} > 800$ GHz
2000	III-V HBT with $f_{\max} > 1$ THz
2007	Indium Phosphide (InP) HEMT with $f_{\max} > 1$ THz
2013	HBT Technology with $f_{\max} = 1.00$ THz
2016	HBT Technology $f_{\max} = 1.15$ THz

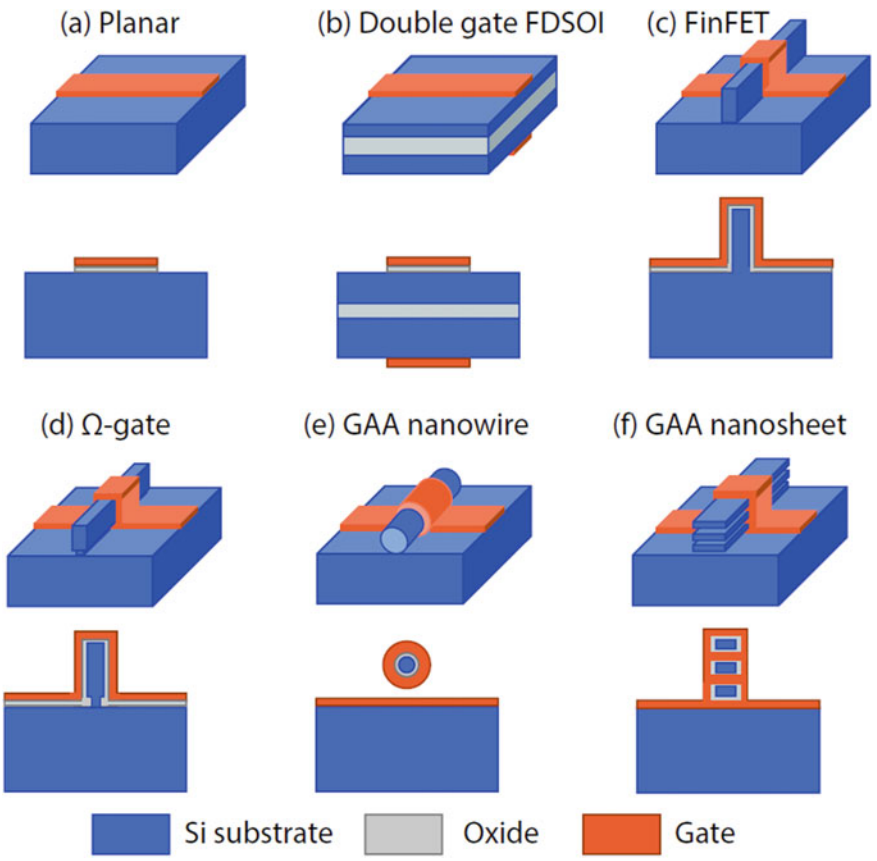

Fig. 1.3 Evolution of MuGFETs from the planar device to the stacking structures. **a** Planar MOSFET. **b** Double-gate (DG) fully depleted SOI MOSFET. **c** FinFET. **d** Ω-gate MOSFET. **e** GAA NW MOSFET. **f** GAA multilayer nanosheet MOSFET

Table 1.2 f_t and $f_{\max}$ performance of Si MOSFETs

Type of device	L(nm)	f_t (GHz)	$f_{\max}$ (GHz)	Year
nMOSFET	29	360	420	2006
nMOSFET	33	270	300	2005
nMOSFET	70	209	248	2004
pMOSFET	29	238	295	2006
Bulk CMOS	45	280	350	2007

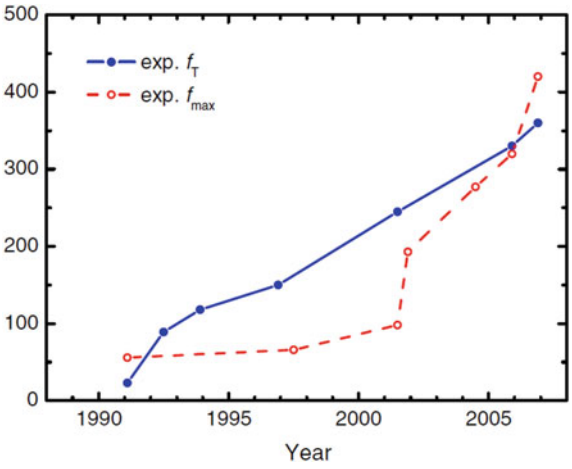

Fig. 1.4 Evolution of the record f_t and f_{max} of RF Si MOSFETs versus time

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Chapter 2
Radio Frequency Transistor Stability and Design Challenges

Abstract Radio frequency transistors are active devices capable of amplifying signals at RF range. The RF transistors can operate as low noise and power amplifiers, mixers, oscillators, frequency converters, etc. RF transistors in general can be divided into two groups: small-signal low-noise transistors and power transistors. For low-noise transistors, low noise and high operating frequency are desired, while power transistors are designed for high output power at high operating frequency. In this chapter, the figure of merit of RF transistor and stability analysis of transistor is discussed. The design challenges of transistors for RF applications are presented.

Keywords RF transistor · Stability · Stability circle · Design challenges

2.1 Introduction

An active device with positive feedback and proper phase can be transformed into an oscillator. This positive feedback could be triggered intentionally or unintentionally, such as by using bias circuits at different levels, forming loops by parallel devices, and using weak isolation among the amplifier stages. These oscillations are categorized into five groups in RF amplifiers: odd mode, even mode, low frequency, parametric and spurious parametric. Design with relatively smaller transistors is necessary for stability analysis of the oscillations in even mode for low noise amplifiers. For both odd mode and even mode, the power amplifier configuration must be stable. Even mode oscillations can arise if a transistor is not unconditionally stable. The stability of the even mode against the oscillations can be reviewed with the help of the two-port network equivalent circuit (EC) model or S-parameters. Calculating stability using an EC model is user-oriented since the device parameters like transconductance and capacitance can be conveniently varied to verify the stability of the transistor. Further, the stability criterion is defined in terms of Rollett condition, K using S-parameters. The importance of the Rollett condition, K is, that it defines whether the active device is unconditionally stable for all passive components.

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2.2 RF Transistors—Figures of Merit (FoM)

RF transistors are active devices that are capable of operating and amplifying signals at RF frequency ranges. The RF transistors can be operated as low-noise and power amplifiers, mixers, oscillators, frequency converters, etc., and it differs from application to application. RF transistors in general can be divided into two groups: small-signal low-noise transistors and power transistors. For low-noise transistors, very low noise in the transistor and high operating frequency is desired, while power transistors are designed for high output power at a high operating frequency. The capabilities and performance of the RF transistor can be assessed through FoM. It is the number or quantity which provides information to device designers for evaluating the device performance and comparing the advantage of different types of transistors. The following are some RF FoM that help to design the transistors for high-frequency applications.

2.2.1 Stability

RF transistors are said to be unconditionally stable at any operating frequency above critical frequency (f_k). The f_k is obtained as the frequency at which stability factor $K = 1$. The device will not oscillate independently from any passive termination network at the transistor's input and output when it is unconditionally stable. However operating frequencies below f_k, the transistor is said to be conditionally stable and certain termination conditions can cause oscillations. The stability behavior of transistor can be described by the stability factor K as introduced by Rollett (1962)

$$K = \frac{2\,\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})}{|y_{12}y_{21}|} \tag{2.1}$$

where y_{11}, y_{12}, y_{21}, and y_{22} are frequency-dependent Y-parameters of the transistor and Re denotes the real part of the quantity in brackets. If $K > 1$, the transistor is unconditionally stable, and for $K < 1$, it works in the region of conditional stability where unintended oscillations may occur.

2.2.2 Cut-Off Frequency ($\mathbf{f_t}$)

Cut-off frequency is defined as the transition frequency at which small-signal current gain drops to unity $|Y_{21}/Y_{11}| = 1$. It is a measure of the maximum useful frequency of a transistor when it is used as an amplifier. Cut-off frequency f_t can be obtained by

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{2.2}$$

2.2.3 Maximum Oscillation Frequency ($\mathbf{f}_{max}$)

The cut-off frequency is surely a good indicator of the low-current forward transit time. However, as a performance indicator, it does not include the effects of gate resistance R_g, which are very important in determining the transient response of a transistor. So an indicator including R_g effects has been proposed. The maximum oscillation frequency is the frequency at which the unilateral power gain roll-off to unity and can be expressed as

$$f_{\max} = \frac{f_t}{2\sqrt{g_{ds}\left(R_g + R_s\right) + 2\pi f_t R_g C_{gd}}} \tag{2.3}$$

$$\text{Unilateral Gain} = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}} - \text{Re}\left(\frac{S_{21}}{S_{12}}\right)\right|} \tag{2.4}$$

2.3 RF Transistor Stability

2.3.1 Transistor Stability

For the circuit shown in Fig. 2.1, oscillation is possible if either the input or output port impedance has a negative real part; this would then imply that $|\Gamma_{\text{in}}| > 1$ or $|\Gamma_{\text{out}}| > 1$, where $|\Gamma_{\text{in}}|$ and $|\Gamma_{\text{out}}|$ are the input and output reflection coefficient. Because $|\Gamma_{\text{in}}|$ and $|\Gamma_{\text{out}}|$ depend on the source and load matching networks, the stability of the amplifier depends on Γ_S and Γ_L (source and load reflection co-efficient) as presented by the matching networks. Thus, we define two types of stability:

1. *Unconditional stability:* The network is unconditionally stable if $|\Gamma_{\text{in}}| < 1$ and $|\Gamma_{\text{out}}| < 1$ for all passives source and load impedances (i.e., $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).
2. *Conditional stability*: The network is conditionally stable if $|\Gamma_{\text{in}}| < 1$ and $|\Gamma_{\text{out}}| < 1$ only for a certain range of passive source and load impedances. This case is also referred to as potentially unstable.

The stability condition of an amplifier circuit is usually frequency-dependent since the input and output matching networks generally depend on frequency. Thus

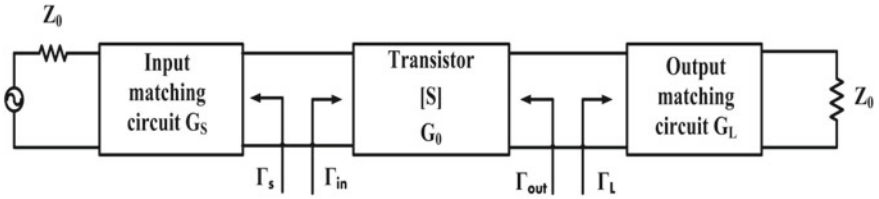

Fig. 2.1 General transistor amplifier circuits

an amplifier can be stable at its design frequency, but unstable at other frequencies. Hence, a careful amplifier design should consider this possibility.

The discussion of stability is limited to two-port amplifier circuits of the type shown in Fig. 2.1, where the S-parameters of the active device can be measured without oscillations over the frequency band of interest. The rigorous general treatment of stability requires that the network S-parameters (or other network parameters) have no poles in the right-half complex frequency plane, in addition to the conditions that $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$.

2.3.2 *Stability Circles*

The following conditions must be satisfied by Γ_S and Γ_L if the amplifier is to be unconditionally stable:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1, \tag{2.5}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{22}\Gamma_S} \right| < 1, \tag{2.6}$$

where $\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$, $\Gamma_s = \frac{Z_S - Z_0}{Z_S + Z_0}$

If the device is unilateral ($S_{11} = 0$), these conditions reduce to the simple results that $|S_{11}| < 1$ and $|S_{22}| < 1$ are sufficient for unconditional stability. Otherwise, the inequalities of Eqs. (2.5) and (2.6) define a range of values for Γ_L and Γ_S where the amplifier will be stable. The range for Γ_L and Γ_S can be obtained by using the Smith chart, and plotting the input and output stability circles. The stability circles are defined as the loci in the Γ_L (or Γ_S) plane for which $\Gamma_{in} = 1$ ($\Gamma_{out} = 1$). The stability circles then define the boundaries between stable and potentially unstable regions of Γ_L and Γ_S. Γ_L and Γ_S must lie on the smith chart ($|\Gamma_S| < 1, |\Gamma_L| < 1$ for passive matching networks).

The equation for the output stability circle can be derived as follows. By using Eq. (2.5) to express the condition that $\Gamma_{in} = 1$ as

$$\left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| = 1, \tag{2.7}$$

or

$$|S_{11}(1 - S_{22}\Gamma_L) + S_{12}S_{21}\Gamma_L| = |1 - S_{22}\Gamma_L|$$

Now define Δ as the determinant of the scattering matrix:

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.8}$$

Then we can write the above result as

$$|S_{11} - \Delta\Gamma_L| = |1 - S_{22}\Gamma_L| \tag{2.9}$$

Now square both sides and simplify to obtain

$$|S_{11}|^2 + |\Delta|^2|\Gamma_L|^2 - \left(\Delta\Gamma_L S_{11}^* + \Delta^*\Gamma_L^* S_{11}\right) = 1 + |S_{22}|^2|\Gamma_L|^2 - (S_{22}^*\Gamma_L^* + S_{22}\Gamma_L$$

$$\left(|S_{22}|^2 - |\Delta|^2\right)\Delta\Gamma\Gamma_L^* - (S_{22} - \Delta S_{11}^*)\Gamma_L - (S_{22}^* - \Delta S_{11}^*)\Gamma_L^* = |S_{11}|^2 - 1$$

$$\Gamma_L\Gamma_L^* - \frac{\left(S_{22} - \Delta S_{11}^*\right)\Gamma_L + (S_{22}^* - \Delta^* S_{11})\Gamma_L^*}{|S_{22}|^2 - |\Delta|^2} = \frac{|S_{11}|^2 - 1}{|S_{22}|^2 - |\Delta|^2} \tag{2.10}$$

Next, complete the square by adding $\left|S_{22} - \Delta S_{11}^*\right|^2 / \left(|S_{22}|^2 - |\Delta|^2\right)\Big)^2$ to both sides.

$$\left|\Gamma_L - \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2}\right|^2 = \frac{|S_{11}|^2 - 1}{|S_{22}|^2 - |\Delta|^2} + \frac{|S_{22} - \Delta S_{11}^*|^2}{\left(|S_{22}|^2 - |\Delta|^2\right))^2},$$

$$\text{or} \quad \left|\Gamma_L - \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2}\right| = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \tag{2.11}$$

In the complex Γ plane, an equation of the form $|\Gamma| = R$ represents a circle with a center at C (a complex number) and a radius of R (a real number). Thus, Eq. (2.11) defines the output stability circle with a center C_L and radius R_L, where

$$C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2}, \text{ (center)}, \tag{2.12}$$

$$R_L = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right|, \text{ (radius)}, \tag{2.13}$$

Similar results can be obtained for the input stability circle by interchanging S_{11} and S_{22}

$$C_S = \frac{\left(S_{11} - \Delta S_{22}^*\right)^*}{|S_{11}|^2 - |\Delta|^2}, \text{(center)}, \tag{2.14}$$

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|, \text{(radius)}, \tag{2.15}$$

Given the S-parameters of the transistor, the input and output stability circles are plotted to define where $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$. On one side of the input stability circle shows $|\Gamma_{\text{out}}| < 1$, while on the other side it shows $|\Gamma_{\text{out}}| > 1$. Similarly, $|\Gamma_{\text{in}}| > 1$ on one side of the output stability circle, and $|\Gamma_{\text{in}}| > 1$ on the other side. From the Smith chart, the stable region can be determined for which $|\Gamma_{\text{in}}| < 1$ and $|\Gamma_{\text{out}}| < 1$.

The output stability circles plotted in the Γ_L plane for $|S_{11}| < 1$ and $|S_{11}| > 1$, as shown in Fig. 2.2. If we set $Z_L = Z_0$, then $\Gamma_L = 0$, and Fig. 2.2a shows that $|\Gamma_{\text{in}}| = |S_{11}|$. Now if $|S_{11}| < 1$, then $|\Gamma_{\text{in}}| < 1$, so $\Gamma_L = 0$ must be in a stable region. This means that the center of the Smith chart ($\Gamma_L = 0$) is in the stable region, so all of the Smith chart ($|\Gamma_L| < 1$) that is exterior to the stability circle defines the stable range for Γ_L.

This region is shaded in Fig. 2.2a. Alternatively, if we set $Z_L = Z_O$ but have $|S_{11}| > 1$, then $|\Gamma_{\text{in}}| > 1$ for $\Gamma_L = 0$, and the center of the Smith chart must be in an unstable region. In this case, the stable region is the inside region of the stability circle that intersects the Smith chart, as illustrated in Fig. 2.2b. Similar results can be applied to the input stability circle.

If the device is unconditionally stable, the stability circles must be completely outside (or enclose) the Smith chart. This result can be expressed as

$$|C_L| - R_L > 1 \text{ for } |S_{11}| < 1 \tag{2.16}$$

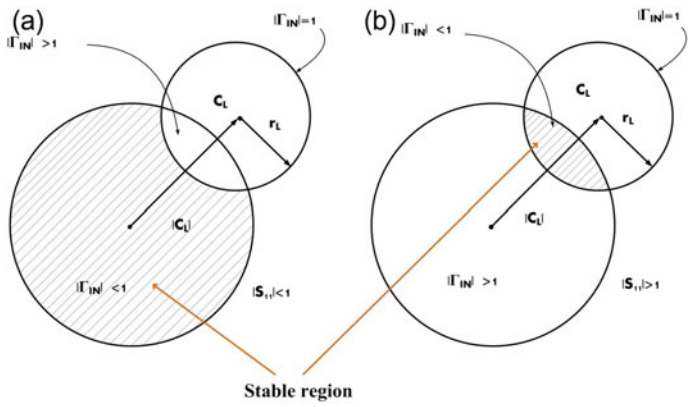

Fig. 2.2 Output stability for unconditionally stable device **a** $|S_{11}| < 1$ **b** $|S_{11}| > 1$

$$|C_s - R_s| > 1 \text{ for } |S_{22}| < 1 \tag{2.17}$$

If $|S_{11}| > 1$ or $|S_{22}| > 1$, the amplifier cannot be unconditionally stable because we can always have a source or load impedance of Z_0 leading to $\Gamma_S = 0$ or $\Gamma_L = 0$, thus causing $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. If the device is only conditionally stable, operating points for Γ_S and Γ_L must be chosen in stable regions, and it is good practice to check the stability at several frequencies near the design frequency. If it is possible to accept a design with less than maximum gain, a transistor can usually be made to be unconditionally stable by using resistive loading.

2.3.3 *Tests for Unconditional Stability*

The stability circles discussed in the previous section can be used to determine regions for Γ_S and Γ_L where the circuit will be conditionally stable, but simpler tests can be used to determine unconditional stability. One of these is the K–Δ test, where it can be shown that a device will be unconditionally stable if Rollet's condition, defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.18}$$

along with the auxiliary condition that

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.19}$$

are simultaneously satisfied. These two conditions are necessary and sufficient for unconditional stability and can be evaluated. If the device S-parameters do not satisfy the K–Δ test, the device is not unconditionally stable, and stability circles must be used to determine if there are values of Γ_S and Γ_L for which the device will be conditionally stable. Also, recall that we must have $|S_{11}| < 1$ and $|S_{22}| < 1$ if the device is to be unconditionally stable.

While the K–Δ test of Eqs. (2.18) and (2.19) is a mathematically rigorous condition for unconditional stability, it cannot be used to compare the relative stability of two or more devices since it involves constraints on two separate parameters.

Recently, a new criterion has been proposed (Marion Lee Edwards 1992) that combines the S-parameters in a test involving only a single parameter, μ, defined as

$$\mu = \frac{1 - |S_{11}|^2}{\left|S_{22} - \Delta S_{11}^*\right| + |S_{12}S_{21}|} > 1 \tag{2.20}$$

Thus, if $> \mu$ 1, the device is unconditionally stable. In addition, it can be said that larger values of μ imply greater stability.

The K–Δ test of Eqs. (2.18–2.19) can be derived from a similar starting point, or more simply from the μ-test of (2.20). Rearranging (2.20) and squaring gives

$$|S_{22} - \Delta S_{11}{}^*|^2 < \left(1 - |S_{11}|^2 - |S_{12}S_{21}|\right)^2 \tag{2.21}$$

It can be verified by the direct expansion that

$$|S_{22} - \Delta S_{11}{}^*|^2 = |S_{12}S_{21}|^2 + \left(1 - |S_{11}|^2\right)\left(|S_{22}|^2 - \left|\Delta^2\right|\right),$$

so Eq. (2.21) expands to

$$\begin{aligned} &|S_{12}S_{21}|^2 + \left(1 - |S_{11}|^2\right)\left(|S_{22}|^2 - \left|\Delta^2\right|\right) \\ &< \left(1 - |S_{11}|^2\right)\left(1 - |S_{11}|^2 - 2|S_{12}S_{21}|\right) + |S_{12}S_{21}|^2. \end{aligned}$$

Simplifying gives

$$|S_{22}|^2 - \left|\Delta^2\right| < 1 - |S_{11}|^2 - 2|S_{12}S_{21}|,$$

which yields Rollet's condition after rearranging:

$$\frac{1 - |S_{11}|^2 - |S_{22}|^2 + \left|\Delta^2\right|}{2|S_{12}S_{21}|} = K > 1. \tag{2.22}$$

In addition to Eq. (2.18), the K–Δ test also requires an auxiliary condition to guarantee unconditional stability. Although the derived Rollet's condition from the necessary and sufficient result of the μ-test, the squaring step used in Eq. (2.21) introduces an ambiguity in the sign of the right-hand side, thus requiring an additional condition. This can be derived by requiring that the right-hand side of Eq. (2.21) be positive before squaring. Thus,

$$|S_{12}S_{21}| < 1 - |S_{11}|^2 \tag{2.23}$$

Because similar conditions can be derived for the input side of the circuit, we can interchange S_{11} and S_{22} to obtain the analogous condition that

$$|S_{12}S_{21}| < 1 - |S_{22}|^2 \tag{2.24}$$

Adding these two inequalities gives

$$2|S_{12}S_{21}| < 2 - |S_{11}|^2 - |S_{22}|^2 \tag{2.25}$$

From the triangle inequality, we know that

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \leq 1 - |S_{11}S_{22}| + |S_{12}S_{21}|,$$

so we have that

$$|\Delta| < |S_{11}||S_{22}| + 1 - \frac{1}{2}|S_{11}|^2 - \frac{1}{2}|S_{22}|^2 < 1$$
$$-\frac{1}{2}\left(|S_{11}|^2 - |S_{22}|^2\right) < 1,$$

this is identical to Eq. (2.19).

2.4 Design Challenges of Transistors for RF Applications

Even most digital systems are benefited gradually from CMOS scaling based on Moore's law but pose various challenges with CMOS implementation in RF and mixed-signal designs. Figure 2.3 depicts the standard integrated RF framework, featuring main subsystems, such as switches, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), frequency synthesizers, power amplifiers, mixers, low noise amplifiers (LNAs), and baseband processors (Jan et al. 2010). Table 2.1 illustrates the different RF devices along with the capabilities such as cutoff frequencies, output resistance, device matching, stability, linearity, and thermal and flicker noise. Hence, the requirements for digital system design are quite different from that of analog systems, and there is a need for different optimization processes and design methodologies (Jan et al. 2010). In this section, conventional transistor design challenges are discussed for RF applications.

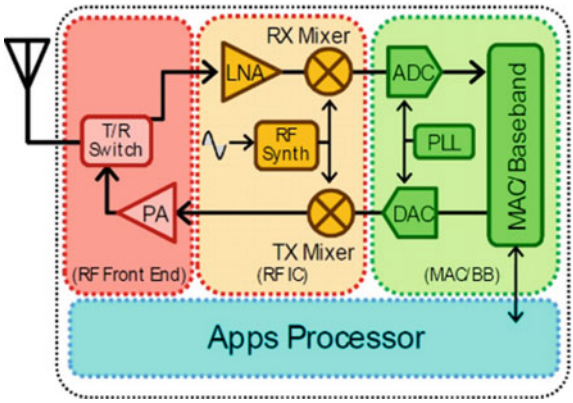

Fig. 2.3 Integrated RF framework, showing key sub systems

Table 2.1 Various RF devices used in RF circuits along with their capabilities

RF devices	RF circuits	Key device characteristics
Logic transistor	MAC/BB, ADC, DAC	I_{dsat}, I_{dlin},Vt, I_{off}
Analog transistor	ADC, DAC, MAC/BB	g_m, R_{out}, Matching, Linearity, Noise, NF_{min}
RF transistor	PA, Mixer, T/R Switch	f_t,f_{max}, 1/f Noise, NF_{min}, Stability
PA transistors	PA	R_{on}, Linearity, f_t,f_{max}, Efficiency, Breakdown V,
Precision resistors	ADC, DAC, BB, Filter, others	R, σR/R, matching
Linear capacitors	PLL, VCO	C, Q, matching
Varactors	PLL, VCO	Tuning ratio, Q, K_{vco},
Inductor/Transformer/Balun	PA, LNA, Mixer	L, Q

2.4.1 Issues Associated with RF FoM

The major challenges encountered while designing the RF transistor associated with RF FOM include realizing the short-gate FETs with optimum RF performance, and suppressing the short channel effects (SCEs) (e.g., poor saturation of $I_{DS}-V_{DS}$ characteristics will lead to large output conductance). More importantly, the advantage of a short gate is compensated by the SCEs and degrades RF performance. Moreover, there is uncertainty regarding the attainment of targeted f_t and f_{max} for short-gate Si MOSFETs (Schwierz and Liou 2007). The result shown in Fig. 2.4 signifies that the parasitics components which could adversely affect the frequency performance have been completely ignored or overlooked. The impact of parasitics (contact/series resistances, stray/fringe capacitance) on the device performance is pronounced more with the scaling of the transistor. From the literature, it is known that in smaller devices, the parasitic resistance, as well as gate fringing capacitance, may have a significant effect on the performance of the transistor (Thompson et al. 2005). Figure 2.4. shows the measured data of f_t and f_{max} with gate length for Si MOSFETs, and it is observed that the device with considerably longer gate length nearly followed the straight line. From the plot, it is also evident that the curves flatten for Si MOSFETs when gate length falls under 100 nm, which is because of SCEs, parasitic resistances, and capacitance start dominating the device performance. Further, the ITRS 2005 targets a linear nature of log (f_t,f_{max})-L for 11 nm gate length Si MOSFETs, which is still a challenging issue.

Ellinger et al. (2011) reviewed the advanced CMOS technologies for RF circuit design and the key finding is, that using only f_t as a benchmarking parameter becomes irrelevant and inaccurate in the case of analog/RF circuit design. Hence, to characterize a technology, in addition to f_t, at least one more parameter, the intrinsic gain (g_m/g_{ds}), should be used. Even f_{max} can be used as a performance parameter since

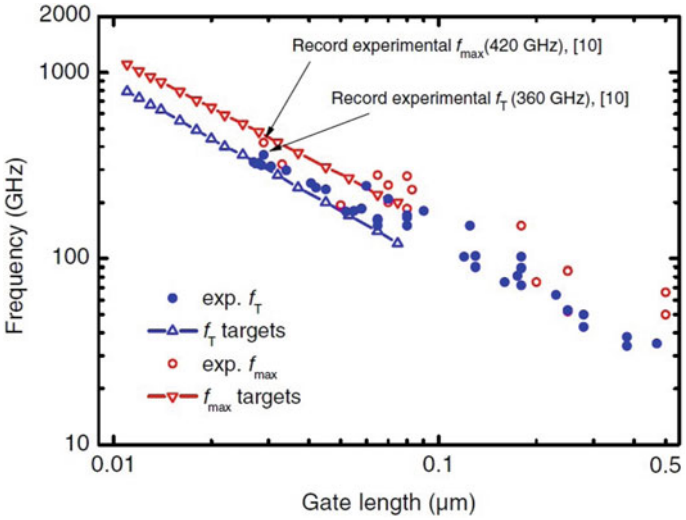

Fig. 2.4 Variation of f_t and $f_{\max}$ with gate length (experimental) and variation of f_t and $f_{\max}$ ITRS 2005 targets for Si MOSFETs

it incorporates all the transistor parasitics and does not have any undesirable terminations. Figure 2.5 presents typical transistor parameters with scaling of CMOS from 350 nm (1997) to 10 nm (projected around 2020). Up to the 350 nm node, the following scaling: $f_t \approx g_m/2\pi C_{gg}$, $\approx Lg^{-2}$ can be applied, where g_m is the transconductance, C_{gg} represents total gate capacitance, and L_g represents the length of the gate.

Scaling the L_g by a factor of two led to an increase of f_t by a factor of four. At 45 nm, the scaling of f_t with L_g has degraded to $\approx L_g^{-1}$ due to SCEs and velocity saturation effects at higher electrical fields. So the f_t has only doubled when the L_g is scaled from 90 to 45 nm. Further scaling from 45 to 10 nm, the impact of L_g on f_t is reduced with the $\approx L_g^{-x}$ where x lies in the range of $0 < x < 1$. Unfortunately, when L_g *is* scaled from 250 to 45 nm, an increase in g_{ds} has to lead to the decrease of intrinsic gain g_m/g_{ds} from 15 to 5. If this progression prolongs, then extrapolation of L_g at 10 nm will yield a unity intrinsic gain and which is not desirable for the design of any RF amplifier. Further from a fabrication point of view, it is very critical too, since the 10 nm technology node needs an oxide thickness t_{ox} of 1 nm to enable adequate gate control over the channel. As 1 nm refers to only a few atomic layers, any scaling of t_{ox} further results in process variation complexities and also increases the gate leakage.

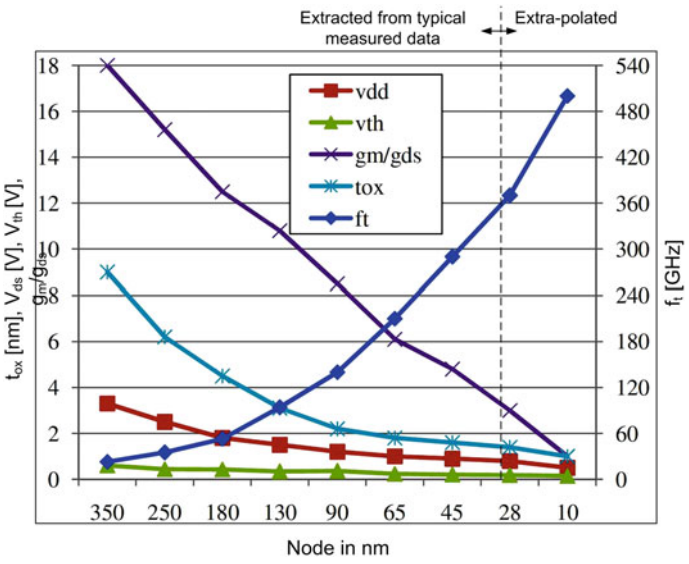

Fig. 2.5 Major transistor performance parameters with CMOS generations

2.4.2 RF Modeling and Characterization

Technologically, it is very difficult to produce reliable and efficient devices below 20 nm channel length. There is a requirement to reduce the device resistance and capacitance to the level of small transistors and thereby improving the usable area of the transistor. In addition to this, there is also a need for modeling and characterization tools for accurate simulation of the devices (Tinoco and Raskin 2010).

Measured scattering or S-parameters are used to model and characterize the active devices at high frequencies, which is of primary importance. Polynomial and physical-based small-signal models are the two different models used in general practice. Polynomial models utilize mathematical optimizations to characterize the MOSFET's behavior as black boxes. These models are quite simple; however, they do not provide details regarding the physical nature of the transistor. Whereas the physical-based small-signal models characterize the MOSFETs behavior in terms of its equivalent electrical circuit's model. The elements of these models have a physical-based origin, but it is very difficult to extract from the measurements. The physical-based small-signal equivalent circuits are used to determine the methodologies and techniques for circuit design or used to determine the impact of each parameter on the dynamic performance of the device.

2.4.3 Critical RF Building Blocks

LNA is a key element in a radio receiver that is used in 3G and 4G cellular applications. It is required to select a technology and circuit topology resulting in high linearity as well as low noise figures. LNAs play a crucial role in the efficiency of radio receivers. Receiver selectivity, sensitivity, and proclivity to absorption of errors will act as measuring parameters for the success of a receiver's design. The RF design engineer optimizes the receiver front-end performance with the focus primarily on the active device. Gain, linearity, noise figure, bandwidth, stability, and dynamic range are the characteristics of LNA design, which are under the control of the designer and have a tendency to impact the receiver sensitivity. To design an amplifier with optimum performance requires the controlling of these characteristics and also an understanding of the behavior of the active device, its impedance matching, and details of the fabrication.

Figure 2.6 represents the variables at the device level and board level that affect LNA performance. To optimize the receiver selectivity and sensitivity and to maintain the integrity of the information, the designer has to reduce the impact of environmental variables with the best trade-off between competing characteristics (Ellinger et al. 2011). Scaling the size of the transistor reduces power consumption, at the expense of noise factor degradation, minimum noise figure ($NF_{\min}$), and third-order intercepts point IP_3 performance. To deliver the best noise figure, a commonly employed common-source transistor in amplifiers is scaled, but this increases the sensitiveness with bias, component tolerances, and temperature. Therefore, there is less scope for a transistor to have its unique value of the normalized input admittance at which the noise factor is at a minimum (Y_{opt}) coincide with the normalized input admittance for maximum power transfer (Y_{in}) or the system's characteristic admittance, Y_o. To minimize the external noise, there is a need for the matching circuit components, so it is required to manipulate the transistor construction (finger dimension, gate finger multiples, layout, and interconnects), RF feedback, and package parasitics. At high frequencies inserting source degeneration feedback results in improved amplifier linearity and stability but reduces the gain. The stability and reliability performance of the device degrade without proper feedback, so the LNA designer looks for the optimal value.

The noise factor of the MOSFET is determined mainly by the gate resistance and the f_t of the device. As the technology scales down to shorter gate lengths, an increase in gate resistance results in a noise factor close to unity. Scaling down the gate length will deteriorate the optimum source impedance and in turn the noise factor in a practical circuit. The later increases as the length of the gate shrinks, which might not be feasible with practical circuit elements. Further scaling in CMOS technology below 45 nm results in high intrinsic f_t of the device, and at low microwave frequencies, the noise factor is dominated by extrinsic parasitics. From Eq. 2.26, the optimum source impedance of the common-source MOSFET is frequency-dependent, which resulted in the increased design complexity of the broadband LNAs. Besides this, any intrinsic limits can also affect the linearity performance of the single FET LNA.

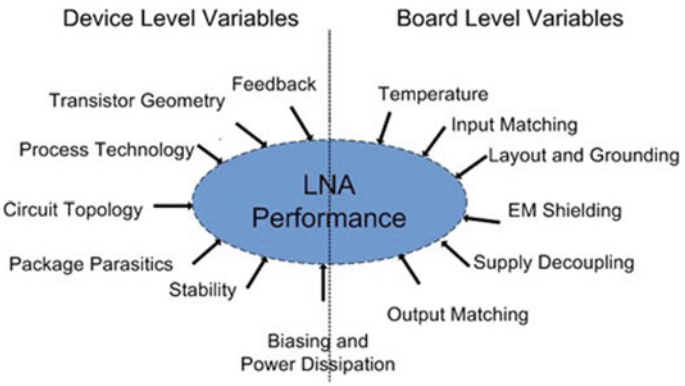

Fig. 2.6 LNA performance variables

Moreover, the linearity performance of the device is limited at higher frequencies due to nonlinear stored charge effects and frequency varying impedance at each terminal. Thus, these effects induce a strong dependency of nonlinearities on the frequency,

$$R_{s,opt} \approx \sqrt{\frac{R_g f_t}{\gamma g_{ds0} f}} \tag{2.26}$$

2.5 Summary

The theory of RF transistors stability factor and a detailed review of design challenges of various field-effect transistors for RF application are discussed. The impact of physical parameters and intrinsic and extrinsic small-signal parameters on RF performance is significant. Scaling of conventional Si MOSFET will improves switching performance of devices. However, high-frequency behavior of these devices doesn't show much improvement as compared to non-silicon-based devices. Multigate MOSFET can be introduced to reduce short channel effects which exhibit improved performance in the RF range.

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Chapter 3
Radio Frequency Stability Performance of DG MOSFET

Abstract The bias and geometry optimization procedure for the radio frequency stability performance of nanoscale symmetric double-gate metal oxide semiconductor field-effect transistors (DG-MOSFET) are presented. The developed stability model provides relation between geometrical parameter and small-signal parameters which helps in optimizing the DG-MOSFET under RF range. The device parameters are extracted for different bias and geometry conditions through numerical simulation, and the RF figures of merit such as cut-off frequency (ft) and maximum oscillation frequency (fmax), along with stability factor, are calculated for an optimized structure.

Keywords DG-MOSFET · Radio frequency · Stability factor · Small-signal parameter

3.1 Introduction

The downscaling of conventional MOSFETs down to sub-50 nm regime leads to an increase in leakage currents and short channel effects (SCEs) which causes severe problems in switching operations. To have better performance, double-gate MOSFET (DG MOSFET) was proposed which has better SCEs suppression capability, higher current drive, lower leakage current, and better scaling. In recent years, DG MOSFETs have become popular for analog and radio frequency applications due to the volume inversion effect at low gate bias. This chapter presents a stability model and detailed study on bias and geometry optimization procedure for RF stability performance of DG MOSFET.

3.2 Numerical Modeling of DG MOSFET

The numerical simulation tool offers capabilities to analyze how structural factors such as geometry and process conditions influence the electrical behavior of DG MOSFET. Simulation data help in quantifying the details of the behavioral models

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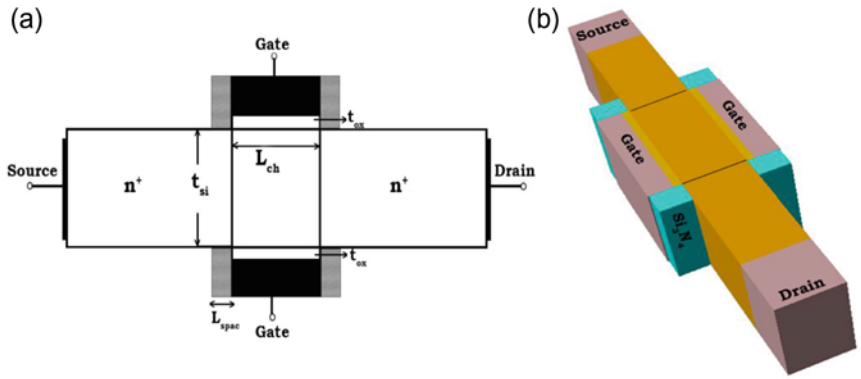

Fig. 3.1 **a** Cross-sectional view and **b** 3-D schematic view of symmetric DG MOSFET

for ICs at the device level and show limitations at the processing and manufacturing levels. Figure 3.1 shows a cross-sectional and 3D schematic view of symmetric DG MOSFET of physical channel length (L_{ch}) of 22 nm and gate oxide thickness (t_{ox}) of 1.6 nm as per the International Technology Roadmap for Semiconductors ITRS (2005). DG MOSFET has an n^+ source and drain with a doping concentration of 2×10^{20} cm^{-3} and channel doping of 10^{15} cm^{-3}. Silicon nitride (Si_3N_4) is used as spacer material which provides mechanical strength. Hafnium oxide (HfO_2) is used as gate dielectric which reduces gate tunneling leakage current and the gate electrode's work function is considered as 4.15 eV. For DC and AC analysis, the electric field-dependent carrier mobility with velocity saturation, band gap narrowing, Lombardi constant voltage and temperature (CVT) along with concentration-dependent mobility model were included for simulation. Fermi–Dirac statistics, Shockley–Read–Hall, and auger recombination for minority carrier recombination have been used along with the density gradient quantum correction model for inversion layer quantum effects for numerical simulation using technology computer-aided design (TCAD) tools.

3.3 Stability Factor Modeling

The stability factor indicates whether the device operates in a stable region at RF frequency range. The DG MOSFET shown in Fig. 3.1 is said to be unconditionally stable at any operating frequency above critical frequency (f_k). The f_k is obtained as the frequency at which stability factor $K = 1$. The device will not oscillate independently from any passive termination network at the transistor's input and output when it is unconditionally stable. However, operating frequencies below f_k, the transistor is said to be conditionally stable and certain termination conditions can cause oscillations. Hence, the device must satisfy the condition $K > 1$ to be unconditionally stable

Gonzales (1997). The stability factor is calculated using Y-parameters at different frequencies of operation for the DG MOSFET. The stability factor computed by Rollet (1962) in terms of the Y-parameter can be expressed as

$$K = \frac{2\,\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12}Y_{21})}{|Y_{12} \cdot Y_{21}|} \tag{3.1}$$

The symmetric DG MOSFET has three terminals, source, drain, and gate. Here both the gates are tied to form a single-gate terminal. The Y-parameters are considered with intrinsic small-signal parameters of symmetric DG MOSFETs Cho et al. (2011).

$$Y_{11} \approx \omega^2 R_{\mathrm{gd}} C_{\mathrm{gd}}^2 + j\omega\left(C_{\mathrm{gs}} + C_{\mathrm{gd}}\right) \tag{3.2}$$

$$Y_{12} \approx -\omega^2 R_{\mathrm{gd}} C_{\mathrm{gd}}^2 + j\omega C_{\mathrm{gd}} \tag{3.3}$$

$$Y_{21} \approx g_m - \omega^2 R_{\mathrm{gd}} C_{\mathrm{gd}}^2 - j\omega(C_{\mathrm{gd}} + \tau \cdot g_m) \tag{3.4}$$

$$Y_{22} \approx g_{\mathrm{ds}} + \omega^2 R_{\mathrm{gd}} C_{\mathrm{gd}}^2 + j\omega C_{\mathrm{gd}} \tag{3.5}$$

These Y-parameters can be used in Eq. (3.1) to simplify further as

$$K \cong \frac{\omega\left(R_{\mathrm{gs}} g_{\mathrm{ds}} C_{\mathrm{gg}}^2 + 2R_{\mathrm{gd}} g_m C_{\mathrm{gg}} C_{\mathrm{gd}} + C_{\mathrm{gg}}^2\right)}{C_{\mathrm{gd}}\sqrt{2\omega^2 g_m C_{\mathrm{gg}}^2 + g_m^2}} \tag{3.6}$$

where C_{gs} is total gate-to-source, C_{gd} is total gate-to-drain and C_{gg} is total gate capacitances $\left(C_{\mathrm{gg}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}\right)$, g_m is transconductance, g_{ds} drain to source conductance, R_{gs} is gate-to-source resistance, and R_{gd} is gate-to-drain resistance.

The Eq. (3.6) is extended to obtain f_k by substituting $k = 1$ and by making the approximation $\omega^4 R_{\mathrm{gd}}^2 C_{\mathrm{gd}}^4 \ll 1$, $\omega^4 R_{\mathrm{gs}}^2 C_{\mathrm{gs}}^4 \ll 1$ and $\omega^2 \tau_m^2 \ll 1$

$$f_k \cong \frac{f_t N}{\sqrt{g_{\mathrm{ds}} g_m R_{\mathrm{gs}} M^2 + NM\left(g_m R_{\mathrm{gd}} + 1\right)}} \tag{3.7}$$

where $M = \frac{C_{\mathrm{gs}}}{C_{\mathrm{gg}}}$, $N = \frac{C_{\mathrm{gd}}}{C_{\mathrm{gg}}}$, and $f_t = \frac{g_m}{2\pi C_{\mathrm{gg}}}$

The total C_{gs} and C_{gd} without considering overlap capacitance and external fringing capacitance can be calculated as follows, Sarkar (2012):

$$C_{\mathrm{gs}} = C_{\mathrm{gsi}} + C_{\mathrm{fint}} \tag{3.8}$$

$$C_{\mathrm{gd}} = C_{\mathrm{gdi}} + C_{\mathrm{fint}} \tag{3.9}$$

$$C_{\text{fint}} = \left[\frac{W\varepsilon_{\text{si}}}{3\pi}\ln\left(1+\frac{t_{\text{si}}}{2t_{\text{ox}}}\sin\left(\frac{\pi}{2}\frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{si}}}\right)\right)\right] \times \mathrm{e}^{-\left((V_{\text{gs}}-V_{\text{FB}}-2\phi_{\text{f}}-V_{\text{ds}})/(3/2)\phi_{\text{f}}\right)^2} \tag{3.10}$$

where ε_{si} and ε_{ox} are dielectric constant of silicon and oxide; W, $t_{\text{si,}}$ and t_{ox} are the width, thickness of silicon body, and gate oxide thickness, respectively. V_{FB} and ϕ_f are the flat band voltage and Fermi potential, respectively. Equation (3.7) describes the relation between critical frequency, intrinsic small-signal parameters, and cut-off frequency which also gives hint for optimization. It is evident from Eq. (3.7) that M and N values can be adjusted to reduce f_k without f_t degradation. But N is the almost independent parameter on the stability model concerning f_t. The optimization begins with the study of factors related to M and N, especially C_{gs}, $C_{\text{gd,}}$ and C_{gg}. Equations (3.8–3.10) show the bias and geometry dependence on C_{gs} and C_{gd} of DG MOSFET. By adjusting the applied gate, drain bias, and geometrical parameters such as silicon body thickness and spacer length, the DG MOSFET can be optimized for better stability performance.

3.4 Bias Optimization of DG MOSFET: RF Stability Perspective

The optimization of DG MOSFET for different biasing conditions depends on the various parameters as stated in Eqs. (3.7–3.10). In this section, the high-frequency performance of DG MOSFET for the different biasing conditions is discussed.

3.4.1 Optimization of Gate to Source Voltage

The stability factor is calculated from extracted Y-parameters for various applied gate to source voltage (V_{gs}) with drain-to-source voltage (V_{ds}) of 0.8 V which are shown in Fig. 3.2. It is evident from Fig. 3.2 that the DG MOSFET attains unconditionally stable conditions at an earlier frequency for higher gate bias. Further increase in gate bias leads to an increase in the total gate to source and gate to drain parasitic capacitances. Also, the cut-off frequency falls due to g_m, because of mobility degradation at higher gate bias. Equation (3.7) shows the dependency of cutoff frequency and parasitic capacitance on critical frequency.

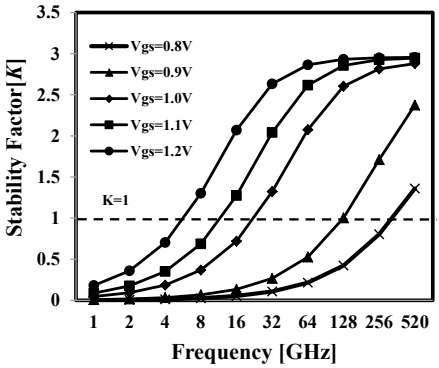

Fig. 3.2 Extracted stability factor for different V_{gs} at V_{ds} = 0.8 V

3.4.2 Optimization of Drain to Source Voltage

The extracted stability factor for various drain biases for a fixed gate bias of 1.2 V is shown in Fig. 3.3. As drain bias increases, the stability performance degrades due to degradation in $C_{gd,}$ and drain-induced barrier lowering (DIBL) affects the device performance at higher drain bias. Hence, smaller drain bias is preferred to operate the DG MOSFET in the RF range.

Figure 3.4 shows the critical frequency as a function of gate bias. The critical frequency reduces with an increase in gate bias and further reduces with a smaller applied drain bias. This shows that at smaller drain bias and higher gate bias, DG MOSFET exhibits better RF stability performance.

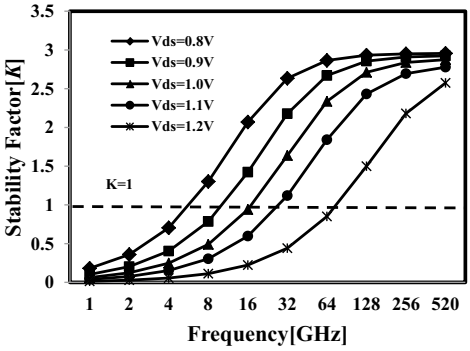

Fig. 3.3 Extracted stability factor for different V_{ds} at V_{gs} = 1.2 V

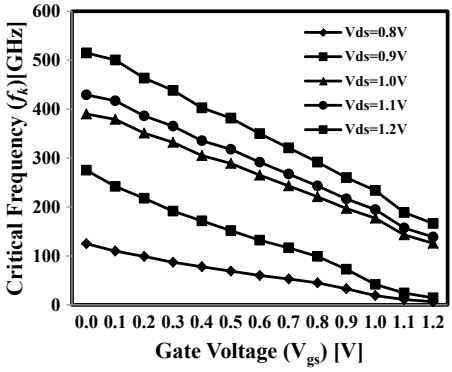

Fig. 3.4 Critical frequency as a function of gate voltage

3.5 Geometry Optimization of DG MOSFET: RF Stability Perspective

The impact of the geometrical parameter is significant on the high-frequency performance of DG MOSFET. It is evident from Eqs. 3.8–3.10 that the capacitance has a direct correlation with the device geometrical parameter such as width of silicon body, thickness of silicon body, and gate oxide thickness. In this section, the optimization strategy of various geometrical parameters of DG MOSFET is discussed.

3.5.1 Optimization of Gate Spacer Length

The gate spacer provides mechanical strength to the gate electrode and also minimizes the fringing field entering to source and drain. Figure 3.5 shows the extracted stability factor and C_{gd} for different spacer lengths (L_{spac}). The L_{spac} has an impact on the RF stability performance of DG MOSFET. The fringing capacitance increases with thinner spacer length thereby causing oscillation at a higher frequency. The variation of spacer length impacts both extrinsic parasitic resistance and fringing capacitance in source and drain regions. The transconductance decreases with an increase in spacer length which leads to degradation in cut-off frequency. The DG MOSFET becomes stable at a critical frequency of 4 GHz for a spacer length of 20 nm as C_{gd} decreases. Further increase in spacer length will not have any impact on stability because C_{gd} saturates for further increase.

Equation 3.7 shows the relation between critical frequency and a small-signal parameter which gives us a guideline for optimizing the suitable value of spacer length without affecting device performance.

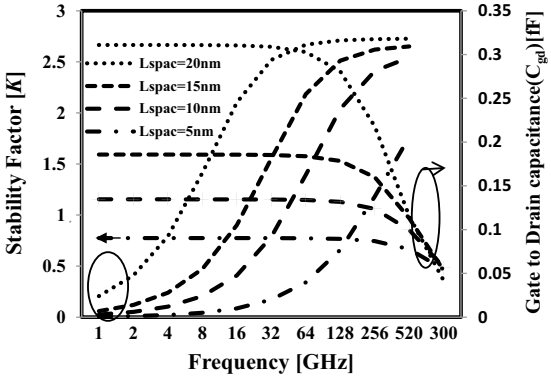

Fig. 3.5 Extracted stability factor and C_{gd} for different spacer lengths

3.5.2 *Optimization of Silicon Body Thickness*

The silicon body thickness has a significant impact on the RF performance of DG MOSFET. Figure 3.6 shows the extracted stability factor and C_{gd} for various silicon body thicknesses (t_{si}). It is evident that for a thinner silicon body, the stability reaches an earlier frequency as compared to a thicker silicon body since C_{gd} decreases with a thinner silicon body. However, silicon body thickness cannot be reduced further because it leads to an increase in device oscillation at a higher frequency. The parasitic source and drain resistance increase with a thinner silicon body which also increases the SCEs. The optimized silicon body thickness for better RF stability is 10 nm which is comparable to the ITRS requirement, ITRS (2005) for ultra-thin silicon body thickness. The silicon body thickness-to-gate length ratio (t_{si}/L_g) was chosen as 0.45 which improves stability performance and should be less than 0.6 for improved SCE suppression.

Equations (3.7–3.10) show the silicon body thickness impact on capacitance through fringing capacitance which provides design guidelines for optimized value of silicon body thickness to operate DG MOSFET at RF range with improved stability performance.

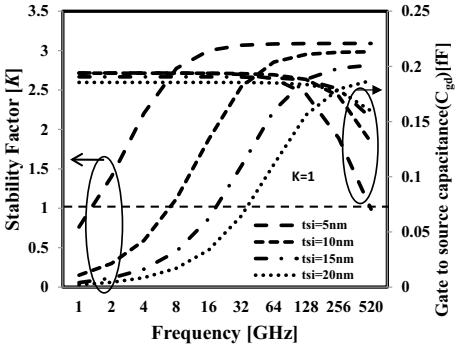

Fig. 3.6 Extracted stability factor and C_{gd} for different silicon body thicknesses

3.6 Optimized Double-Gate MOSFET for Improved RF Stability Performance

It is observed from the detailed study of the previous section that the DG MOSFET exhibits better stability performance for silicon body thickness of 10 nm, oxide thickness of 1.6 nm, and spacer length of 20 nm. Figure 3.7 shows the extracted stability factor for the optimized structure. The stability factor reaches 1 at 7.5 GHz which shows that the device can be operated unconditionally stable and indicates that DG MOSFET does not require an additional stabilization circuit when operated from 7.5 GHz onward in radio frequency integrated circuits. However, below the critical frequency, the DG MOSFET will be potentially or conditionally stable. A suitable device parameter can be chosen for DG MOSFET to make the device to be stable at a particular frequency.

The characteristic frequencies f_t and $f_{\max}$ provide information to device engineers about the capability of DG MOSFET operating at the RF range. The cut-off frequency f_t is evaluated as the frequency for which the magnitude of short circuit gain drops to unity. The f_t is expressed as

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{3.11}$$

The $f_{\max}$ is related to the capability of the device to provide power gain at large frequencies and is defined as the frequency at which the magnitude of the maximum available power gain drops to unity. The $f_{\max}$ is expressed as

$$f_{\max} = \frac{f_t}{\sqrt{4(R_s + R_g + R_i)\left(g_{ds} + 2\pi f_t C_{gd}\right)}} \tag{3.12}$$

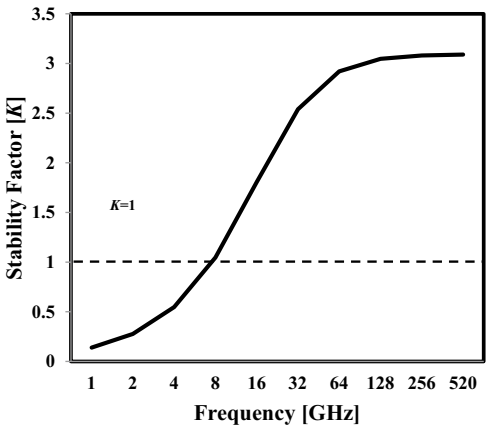

Fig. 3.7 Extracted stability factor for optimized DG MOSFET at $V_{gs} = 1.2$ V and $V_{ds} = 0.8$ V

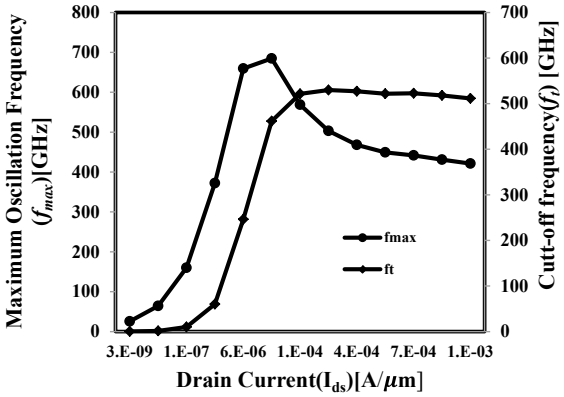

Fig. 3.8 Variation of f_t and $f_{\max}$ with drain current for optimized DG MOSFET at $V_{gs} = 1.2$ V and $V_{ds} = 0.8$ V

Figure 3.8 shows the variation of f_t and $f_{\max}$ with drain current for the optimized DG MOSFET. The bias and geometry optimized structure have f_t of 650 GHz due to the improved g_m and $f_{\max}$ of 700 GHz, which shows that the proposed DG MOSFET structure is suitable for high-speed switching and high-frequency applications.

3.7 Summary

The RF stability model can be developed for DG MOSFET and its stability characteristics can be analyzed using numerical simulation. The device stability was studied for various bias and geometry conditions and observed that, C_{gd} and C_{gs} are responsible for degradation in critical frequency. The proposed optimized geometry and bias condition show excellent stability performance. There is no additional circuit required as the device is unconditionally stable from 7.5 GHz onward.

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Chapter 4
Radio Frequency Stability Performance of Double-Gate Tunnel FET

Abstract The radio frequency stability performance and its impact of parameter fluctuation due to process variation of double-gate tunnel FET (DG TFET) are presented. The influence of parameter fluctuation due to process variation leads to DG TFET performance degradation. The RF figures of merit (FoM) such as cut-off frequency (f_t), maximum oscillation frequency ($f_{\max}$) along with stability factor for different silicon body thickness, gate oxide thickness, and gate contact alignment are obtained from extracted device parameters. The impact of parameter fluctuation of silicon body thickness, gate oxide thickness, and gate contact alignment of DG TFET was found significant, and the design guidelines are provided for RF applications.

Keywords DG tunnel FET · Radio frequency · Process variation

4.1 Introduction

The tunnel field-effect transistor (Tunnel FET) has received much attention for mobile electronic applications which require low-standby-power (LSTP) operation active devices as reported by the International Technology Roadmap for Semiconductor ITRS, (2005) because of its lower off current (I_{off}). Tunnel FETs act as field-effect transistors but use band-to-band tunneling for carrier transport. When the device is turned on, the carriers tunnel through the barrier so that current can flow from source to drain. When the device is off, the presence of the barrier keeps the off-current extremely low; hence, leakage current reduces drastically. High-k gate dielectric increases the current of Tunnel FET and is also added with the bottom gate to double the current Boucart et al. (2007). Many researchers study the fabrication and DC characteristics of Tunnel FET Bjork et al. (2008), Moselund et al. (2009), Moselund et al. (2011). Similarly, many research groups worked on radio frequency (RF) performance of single-gate silicon-on-insulator (SOI) MOSFET, SOI-double-gate (DG) MOSFET, and silicon nanowire FET Eminente et al. (2004), Cerdeira et al. (2010), Sivasankaran et al. (2012). In this chapter, the RF stability performance and impact of process variation on the stability performance of double-gate tunnel FET (DG Tunnel FET) are discussed.

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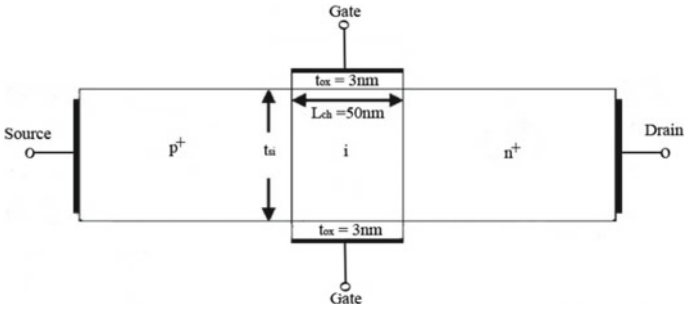

Fig. 4.1 Schematic structure of DG Tunnel FET

4.2 Numerical Modeling of DG Tunnel FET

Numerical modeling has become a useful tool to study the DG Tunnel FET also like other field effect transistors. Numerical modeling using computer-aided design includes a suite of physical models describing carrier transport in devices which helps to understand the electrical behavior of DG Tunnel FET. Let us consider a DG Tunnel FET of physical channel length (L_{ch}) of 50 nm and gate oxide thickness (t_{ox}) of 3 nm as shown in Fig. 4.1. The device has a p^+ source region, an intrinsic p-type channel region, and an n^+ drain region with a uniform doping concentration of 2×10^{20} cm^{-3}, 1×10^{17} cm^{-3}, and 2×10^{20} cm^{-3}, respectively. Hafnium oxide (HfO_2) is used as gate oxide material to reduce the gate leakage current. The source to intrinsic and intrinsic to drain junctions are abrupt. For numerical simulation, band-to-band tunneling (BBT) Kane model with Fermi–Dirac statistics along with constant mobility and Shockley–Read–Hall recombination model need to be activated ATLAS Manual (2012). A very fine mesh is recommended in the tunneling region so that energy band profiles can be accurately determined to calculate the current in that energy range. The DC and AC analysis is performed to extract threshold voltage and to obtain intrinsic and extrinsic parameters of DG Tunnel FET.

4.3 Small-Signal Modelling of DG Tunnel FET

A MOSFET can be considered where the terminal voltage variations are sufficiently small so that the resulting small current variation can be expressed in terms of using linear relations. The circuit developed using the linear relation is called small-signal circuit. The small-signal equivalent circuit is shown in Fig. 4.2. In the circuit, C_{gs} and C_{gd} are intrinsic gate to source and gate to drain capacitances, and R_{gs} and R_{gd} are gate to source and gate to drain resistances which contribute to channel distributed resistance. C_{sdx} is the source to drain capacitance which varies with larger drain

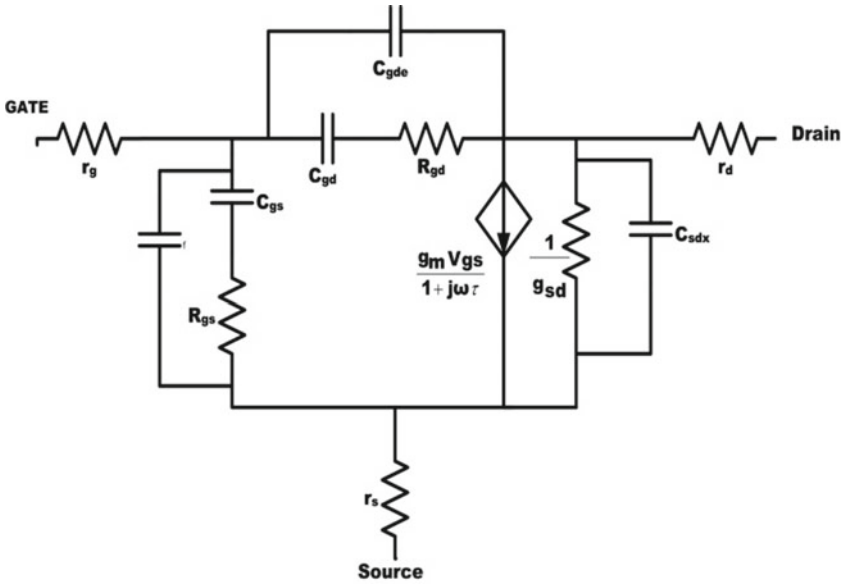

Fig. 4.2 Small-signal non-quasi static model of MOSFET (intrinsic and extrinsic part)

bias on short channel devices. g_m and g_{ds} are transconductance and drain to source conductance, respectively.

R_{gd} C_{gd}, $R_{gs}C_{gs}$, and the time constant τ are responsible for the time delay of the charges in the tunneling region. The effect of the time constant can be formulated using the non-quasi small-signal circuit shown in Fig. 4.2. The Y-parameters are extracted from the intrinsic non-quasi static small-signal equivalent circuit Tsividis (1999) after neglecting extrinsic parameters and are represented as

$$Y_{11} = \frac{j\omega C_{gs} + \omega^2 R_{gs} C_{gs}^2}{1 + \omega^2 R_{gs}^2 C_{gs}^2} + \frac{j\omega C_{gd} + \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \tag{4.1}$$

$$Y_{12} = \frac{-j\omega C_{gd} - \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \tag{4.2}$$

$$Y_{21} = \frac{g_m - j\omega g_m \tau}{1 + \omega^2 \tau^2} - \frac{j\omega C_{gd} + \omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \tag{4.3}$$

$$Y_{22} = \frac{g_{ds} + j\omega g_{ds} R_{gd} C_{gd} + j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \tag{4.4}$$

Using the real and imaginary parts of the Y-parameter, the values of device parameters can be extracted as

$$C_{\mathrm{gd}} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{4.5}$$

$$C_{\mathrm{gs}} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})}{\omega} \tag{4.6}$$

$$R_{\mathrm{gd}} = -\frac{\mathrm{Re}\, Y_{12}}{\omega^2 C_{\mathrm{gd}}^2} \tag{4.7}$$

$$R_{\mathrm{gs}} = \frac{1}{C_{\mathrm{gs}}^2}\left(\frac{\mathrm{Re}(Y_{11})}{\omega^2} - R_{\mathrm{gd}} C_{\mathrm{gd}}^2\right) \tag{4.8}$$

$$g_m = \mathrm{Re}(Y_{21})|\omega^2 = 0 \tag{4.9}$$

$$g_{\mathrm{ds}} = \mathrm{Re}(Y_{22})|\omega^2 = 0 \tag{4.10}$$

$$\tau = -\frac{1}{g_m}\left(\frac{\mathrm{Im}(Y_{21})}{\omega} + C_{\mathrm{gd}}\right) \tag{4.11}$$

$$C_{\mathrm{sdx}} = \frac{\mathrm{Im}(Y_{22})}{\omega} - C_{\mathrm{gd}} \tag{4.12}$$

The above-mentioned parameters were extracted at necessary bias conditions applied to the gate to source voltage (V_{gs}) and drain to source voltage (V_{ds}) terminal of the device. From Eqs. (4.5–4.12), the intrinsic small-signal parameters can be calculated using Y-parameters and the model describes the behavior of DG Tunnel FET at the cut-off frequency. To model the RF behavior over a wide frequency range, it is necessary to calculate the intrinsic capacitances of the DG Tunnel FET. The extracted C_{gs} and C_{gd} as a function of gate voltage (V_{gs}) are shown in Fig. 4.3 at 1 GHz. The C_{gd} is alone responsible for total gate capacitance (C_{gg}) as C_{gs} exponentially decreases as gate voltage increases because of the presence of device potential barrier at the source side and C_{gd} increases with an increase in gate voltage due to the reduction of the potential barrier at the drain side. Hence, the contribution of C_{gd} is more significant in C_{gg}.

The extrinsic parameters gate resistance (r_g), source resistance (r_s), and drain resistance (r_d) can be calculated using extracted Z-parameters from a device operated at $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 0$ V. The equations for the extrinsic parameters, Lovelace et al. (1994), are

$$\mathrm{Re}(Z_{11}) = r_g + r_s \tag{4.13}$$

$$\mathrm{Re}(Z_{22}) = r_d + r_s \tag{4.14}$$

$$\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = r_g \tag{4.15}$$

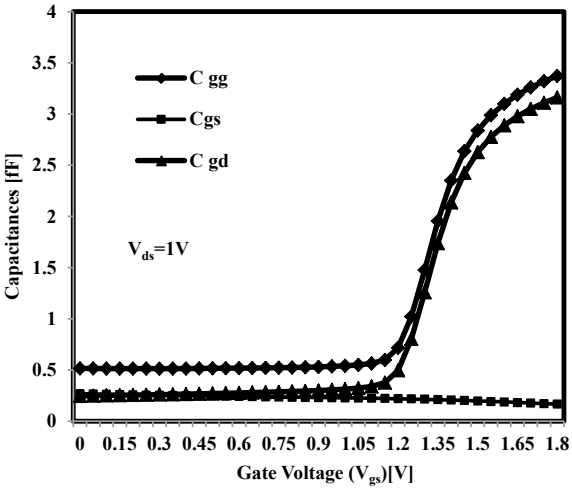

Fig. 4.3 Extraction of C_{gs} and C_{gd} as a function V_{gs} for $V_{ds} = 1$ V

4.4 RF Stability Performance of Double-Gate Tunnel FET

The stability of a device is determined by its stability factor (K), which describes the unstable oscillations due to the input or output impedance of the transistor. The stability parameter, K, indicates whether a device is conditionally/unconditionally stable.

The RF performance of DG Tunnel FET is evaluated by extracting cut-off frequency (f_t), maximum oscillation frequency (f_{max}), g_m, and g_{ds} which are known as Figures of Merit (FoMs). It is necessary to observe the response of these FOMs to understand their behavior at high-frequency ranges. The f_t and f_{max} are the two parameters mainly responsible for estimating the high-frequency performance of RF devices and can be defined as

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{4.16}$$

$$f_{max} = \frac{f_t}{\sqrt{4 \cdot R_g \cdot \left(g_{ds} + 2\pi \cdot f_t C_{gd}\right)}} \tag{4.17}$$

Figure 4.4 shows extracted f_t and f_{max} as a function of gate voltage. The value of f_t decreases when the total gate capacitance increases, and this is more significant in the small channel dimension of DG Tunnel FET. The f_t is extracted when the current gain is unity $|Y_{21}/Y_{11}| = 1$ and it is found to be 350 GHz. From Eq. (4.16), it is observed that f_t increases as transconductance increases and for DG Tunnel FET, the f_t is higher because of higher transconductance. This shows the capability of DG Tunnel FET to operate at higher frequencies. The f_{max} is related to the capability of the device to provide power gain at large frequencies and is defined as the frequency at

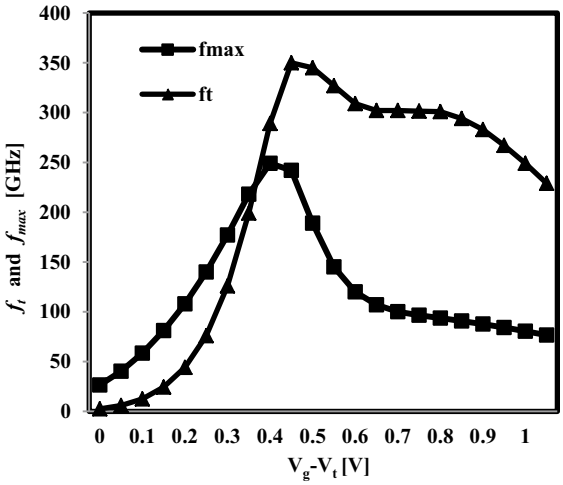

Fig. 4.4 f_t and $f_{\max}$ for different $V_g - V_t$, and $V_{\mathrm{ds}} = 1$ V

which the magnitude of the maximum available power gain is obtained under power-matching conditions at both the input and output ports drops to unity. The obtained f_t and $f_{\max}$ values of DG Tunnel FET are higher as compared to bulk MOSFET, Boucart et al. (2007).

It must satisfy the condition $K > 1$ for a device to be unconditionally stable, Eminente et al. (2004). The stability factor in terms of the Y-parameter can be expressed as

$$K = \frac{2\,\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12} - Y_{21})}{|Y_{12} - Y_{21}|} \tag{4.18}$$

Figure 4.5 shows the extracted stability factor over the frequency range of 1–101 GHz, and it is found that $K > 1$ from 11 GHz onward. When the device is unconditionally stable from 11 GHz onward, it indicates that additional stabilization circuits are not required for RF amplifiers when operating above this frequency, which reduces the circuit complexity. Hence the DG Tunnel FET structure shown in Fig. 4.1 can be operated in high frequency and high-speed applications without oscillations. However, at below 11 GHz, DG Tunnel FET will be conditionally stable; hence, device's small-signal parameter can be chosen so that the device can operate in a stable region at a particular frequency.

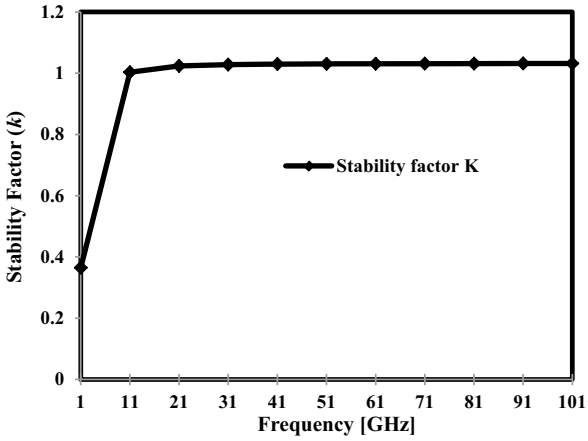

Fig. 4.5 Extracted stability factor of DG tunnel FET as a function of frequency

4.5 Impact of Process Variation on RF Stability Performance of DG Tunnel FET

The process variation is the naturally occurring variation in the attributes of semiconductor transistors width, length, oxide thickness, and doping concentration when integrated circuits are fabricated. The amount of process variation becomes particularly pronounced at smaller process nodes as the variation becomes a larger percentage of the full length or width of the device and as feature sizes approach the fundamental dimensions such as the size of atoms and the wavelength of usable light for patterning lithography masks. In this section, the process variation such as silicon body thickness, oxide thickness, doping concentration, and gate contact alignment effect on the performance of DG Tunnel FET is discussed.

4.5.1 Impact of Body Thickness Variation

The silicon body thickness (t_{si}) becomes important when devices are fabricated on thin substrates to achieve better gate control and reduce capacitive effects. The impact of silicon body thickness on RF performance of DG Tunnel FET is found significant. Figure 4.6 shows the fluctuation of f_t and f_{max} for variation in t_{si} of DG Tunnel FET. The silicon thickness variation (Δt_{si}) is considered as $\pm$ 1, $\pm$ 3 and $\pm$ 5 nm for thickness from 10 to 25 nm. The impact of Δt_{si} at $\pm$ 1 and $\pm$ 3 nm is around 10% of f_t and f_{max} fluctuation ($\Delta f_t/f_t$ and $\Delta f_{max}/f_{max}$). The f_t and f_{max} fluctuation increase as Δt_{si} reaches $\pm$ 3 nm which is predominant for smaller t_{si}. At silicon body thickness of 20 nm and above, the f_t and f_{max} fluctuation is less as compared to smaller t_{si}; however, as per ITRS requirements, the silicon body thickness should be 7 nm for high-performance logic, ITRS (2009). Hence, t_{si} should be kept at 15 nm which is

comparable to the International Technology Roadmap for Semiconductors (ITRS) requirement and restrict Δt_{si} within $\pm$ 3 nm for better RF performance.

The critical frequency (f_k) for various silicon body thicknesses is shown in Fig. 4.7. It is evident that for silicon thickness of 10 nm, the f_k got fluctuated for Δt_{si} of $\pm$ 1, $\pm$ 3 $\pm$ 5 nm. The impact of Δt_{si} is less for large silicon thicknesses. However, to take the advantage of the double gate and to achieve stability of DG Tunnel FET at a smaller frequency, it is suggested to have t_{si} around 15 nm and to keep Δt_{si} within $\pm$ 3 nm.

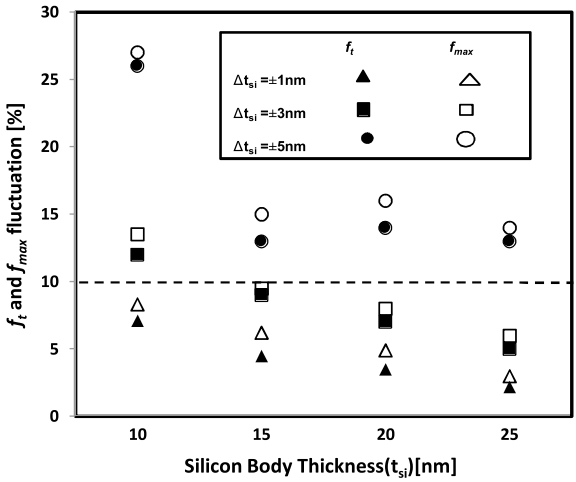

Fig. 4.6 Impact of silicon body thickness variation on f_t and f_{max} of DG Tunnel FET

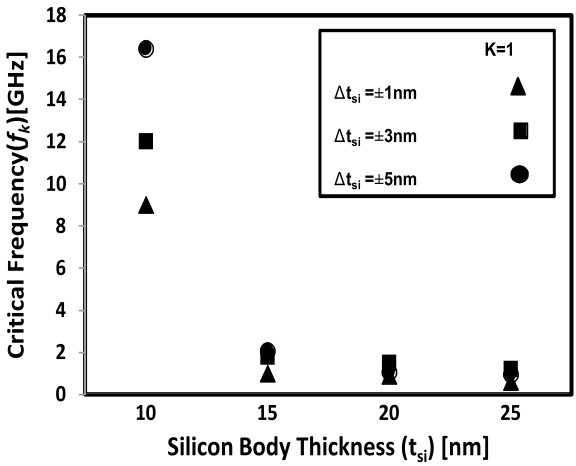

Fig. 4.7 Impact of silicon body thickness variation when keeping $K = 1$ of DG Tunnel FET

4.5.2 Impact of Oxide Thickness Variation

The impact of gate oxide thickness variation on device performance is significant in nanoscale devices. The gate oxide provides capacitive coupling between gate and channel which controls the drain current of DG Tunnel FET. The gate oxide thickness variation (Δt_{ox}) can cause fluctuation in DG Tunnel FET DC characteristics, Boucart et al. (2010). Figure 4.8 shows the impact of gate oxide thickness variation on f_t and f_{max} fluctuations. The f_t and f_{max} fluctuations are less than 10% for Δt_{ox} of $\pm$ 0.2 nm, however, as Δt_{ox} increases to $\pm$ 0.6 nm and $\pm$ 1 nm, the fluctuation is higher because gate capacitance varies with different oxide thicknesses. The RF performance of DG Tunnel FET will not be affected if Δt_{ox} is within $\pm$ 0.2 nm. Hence, it is suggested to control the process variation by better oxidation process and to keep Δt_{ox} less than $\pm$ 0.2 nm.

Figure 4.9 shows the critical frequency for different t_{ox}. The f_k fluctuation for smaller oxide (at $t_{ox} = 1$ nm) thickness is less as compared to larger oxide (at $t_{ox} =$ 4 nm) thickness for Δt_{ox} of $\pm$ 0.2, $\pm$ 0.6 and $\pm$ 1 nm. When t_{ox} is 1 nm, the DG Tunnel FET is unconditionally stable at a critical frequency of 0.5 GHz, this shows the thinner gate dielectric is preferable to operate DG Tunnel FET for better stability under RF range.

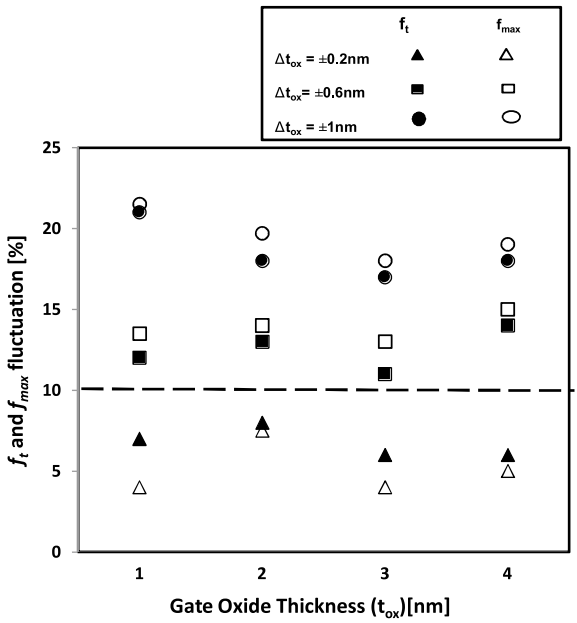

Fig. 4.8 Impact of gate oxide thickness variation on f_t and f_{max} of DG Tunnel FET

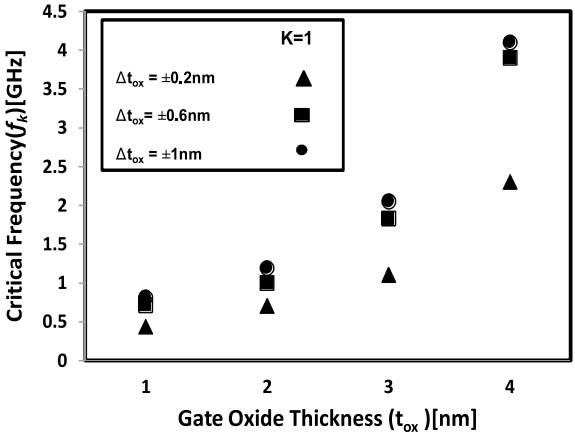

Fig. 4.9 Impact of gate oxide thickness variation when keeping $K = 1$ of DG Tunnel FET

4.5.3 Impact of Gate Contact Alignment

Controlling the source-intrinsic region leads to an increase in DG Tunnel FET speed and reduced fringing field, this can be achieved through gate contact alignment (L_{gca}). Figure 4.1 shows a self-aligned gate structure, the top and bottom gate of DG Tunnel FET can be under-lap (negative gate contact alignment) or overlapped (positive gate contact alignment) on the source-intrinsic region to improve RF performance. Figure 4.10 shows an overlap gate structure on top of the intrinsic source region.

Figure 4.11 shows the impact of gate contact alignment variation (ΔL_{gca}) on f_t and $f_{\max}$ for under-lap (negative alignment values) and overlap (positive alignment values) structures. For ΔL_{gca} of $\pm$ 0.6 nm, the f_t and $f_{\max}$ fluctuation crosses 10% and fluctuation is more for both under-lap and overlap structures as ΔL_{gca} increases. It is recommended to keep the L_{gca} within 10% of channel length and ΔL_{gca} less than $\pm$ 0.2 nm to obtain better RF performance of DG Tunnel FET.

The critical frequency is plotted for various L_{gca} and shown in Fig. 4.12. It is found that the K value reaches 1 at lower frequencies for gate under-lap structure as compared to gate overlap. The gate contact alignment at -10 and -15 nm shows good stability performance. But these alignments cannot provide good DC characteristics, Boucart et al. (2010); Vandooren et al. (2012) and will make the fabrication process difficult. Therefore, it is recommended that the optimal position for gate contact should be within 5 nm for gate under-lap for better stability conditions.

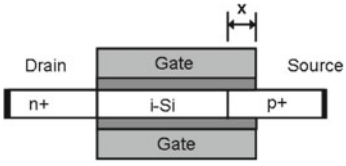

Fig. 4.10 Overlap gate contact alignment of DG Tunnel FET

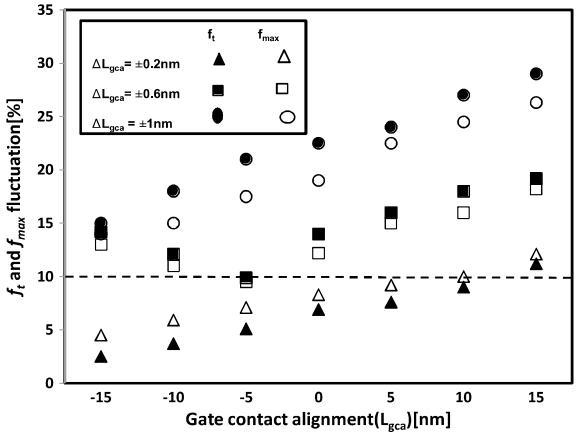

Fig. 4.11 Impact of gate contact alignment variation on f_t and $f_{\max}$ of DG Tunnel FET

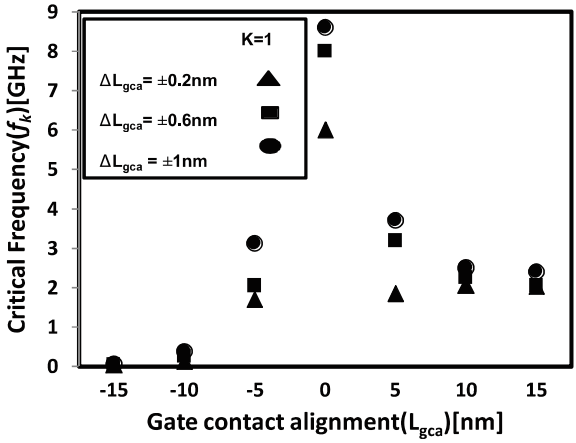

Fig. 4.12 Impact of gate contact alignment variation when keeping $K = 1$ of DG Tunnel FET

4.5.4 Impact of Doping Concentration

The source doping concentration (N_D) has an impact on the device performance since the intrinsic to source region built-in potential depends on the source doping level. The impact of source doping variation (ΔN_D) on f_t and $f_{\max}$ is shown in Fig. 4.13. At each exponential order of N_D such as 1×10^{17}, 1×10^{18}, 1×10^{19} and 1×10^{20} cm^{-3}, the variations are considered as $\pm\ 0.3 \times 10^{\circ}$, $\pm\ 0.6 \times 10^{\circ}$ cm^{-3}, and $\pm\ 1.0 \times 10^{\circ}$ cm^{-3}. The drain doping concentration is assumed as 2×10^{20} cm^{-3}. The f_t and $f_{\max}$ fluctuation crosses 10% for concentration variation of $\pm\ 0.6 \times 10^{\circ}$ cm^{-3}; hence, it is suggested to follow the careful deposition mechanism for source and drain doping.

The critical frequency is plotted for various N_D and shown in Fig. 4.14. It is found that the k value reaches 1 at lower frequencies for the highly doped source

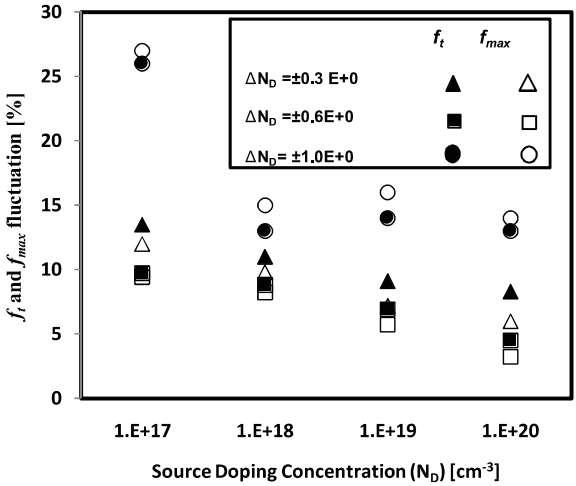

Fig. 4.13 Impact of doping concentration variation on f_t and $f_{\max}$ of DG Tunnel FET

as compared to the lower doped source region. When N_D is higher, the DG Tunnel FET shows good stability performance provided ΔN_D should be within $\pm$ 0.3 $\times$ 10° cm^{-3}. Therefore, it can be suggested that the optimal doping concentration for the source would be in the order of 1 $\times$ 10^{20} cm^{-3} and ΔN_D restricted to $\pm$ 0.3 $\times$ 10° cm^{-3} for better stability conditions.

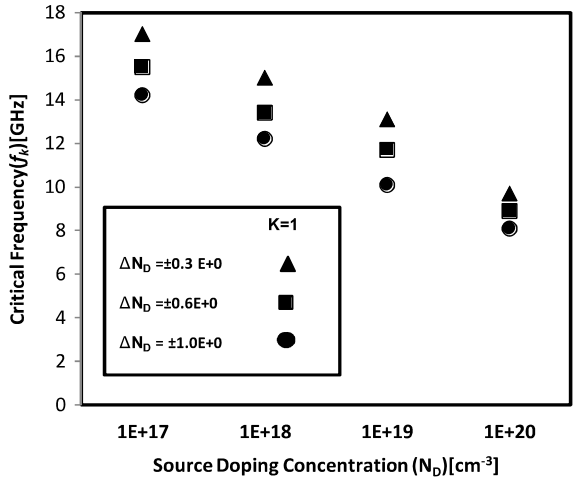

Fig. 4.14 Impact of doping concentration variation when keeping $K = 1$ of DG Tunnel FET

4.6 Summary

The RF stability performance of DG Tunnel FET is discussed. The small-signal parameters of the device are extracted through ac analysis. It is found that the cut-off frequency and the maximum oscillation frequency can be obtained accurately. The study reveals that the impact of process variation is also found obvious in RF stability performance at smaller gate lengths. From the result, we can observe that variation within $\pm$ 3 nm on silicon body thickness $\pm$ 0.3 nm on oxide thickness, $\pm$ 0.2 nm on gate contact alignment, and $\pm$ 0.3 $\times$ 10° cm^{-3} on doping concentration show good RF and stability performance. The optimized parameter values to operate DG Tunnel FET under the RF range are silicon thickness of 15 nm, oxide thickness of 1 nm, and source and drain doping in the order 1 $\times$ 10^{20} cm^{-3} with gate contact alignment of 10% of channel length.

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Chapter 5
Radio Frequency Stability Performance of FinFET

Abstract RF stability of FinFET at particular bias and geometry conditions is presented. The FinFET geometrical parameters such as gate spacer length, height of silicon fin, and thickness of silicon fin along with gate material work function and bias conditions are adjusted to optimize the device for better stability performance at RF range. The critical frequency (f_k) is obtained for different bias and geometry conditions using numerical simulation.

Keywords FinFET · Radio frequency · Stability · Fin height · Fin thickness

5.1 Introduction

A multiple-gate MOSFET device with an ultrathin vertical silicon body, called the "fin," on a silicon pedestal, sidewall gate stack, a source, and a drain at the two ends of the gate length is called the "fin field-effect transistor" or "FinFET." Thus, a FinFET includes an ultrathin vertical silicon fin on a silicon substrate with a thin insulating layer such as silicon dioxide (SiO_2) grown on the sidewalls, a conducting metal layer, called the gate electrode deposited on the top of the gate oxide, and heavily doped source and drain regions formed from one end of the fin to the nearest gate edge and from the far edge of the gate to the far end of the fin, respectively. In reality, the gate can be placed on two, three, or four sides of the channel or wrapped around the channel as discussed in Chap. 1. FinFETs exhibit a better I_{on}/I_{off} ratio and reduced fabrication complexity as compared to other multigate structures Jakub Kedzierski et al. (2004). The fabrication and DC characteristics of FinFETs are reported by Tsormpatzoglou et al. (2009) and Lederer et al. (2005). The capabilities of FinFETs for analog applications are reported by Kilchytska et al. (2004) and Guillorn et al. (2008). The effect of a geometrical parameter such as fin height (H_{fin}), fin width (W_{fin}), fin thickness (T_{fin}), and fin spacing (S_{fin}) on radio frequency (RF) performance of Silicon-on-Insulator (SOI) FinFET was reported earlier by Wu et al. (2007). Similarly, parasitic and geometry optimizations of FinFET for RF applications were studied by Kranti et al. (2008). The impact of extrinsic capacitances on RF performance of FinFET was analyzed using numerical simulation Tinoco (2013). From the analysis, it is found that the extrinsic capacitances are larger than intrinsic

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capacitance which leads to degradation of RF performance. There is a dependency of geometrical parameters on intrinsic and extrinsic capacitances. The FinFET geometrical parameters such as gate spacer length, the height of silicon fin, and thickness of silicon fin along with gate material work function and bias conditions are optimized for better stability performance in the RF range. The guideline for optimizing the FinFET at the RF range is discussed in this chapter.

5.2 Numerical Modeling of FinFET

The FinFET electrical behavior is characterized by numerical modeling using the Technology Computer Aided Design (TCAD) simulator. Figure 5.1a shows the 3D structure of FinFET which has a physical channel length (L_g) of 22 nm ITRS, (2010), gate oxide thickness (t_{ox}) of 1 nm, T_{fin} of 8 nm, and H_{fin} of 24 nm. The device has an n^+ source and drain region and p-type channel region with doping of 1×10^{20} cm^{-3} and 1×10^{16} cm^{-3}, respectively. Hafnium oxide (HfO_2) is used for gate dielectric and silicon nitride (Si_3N_4) for gate spacer. The use of poly-Si electrodes can cause dopant diffusion through high-k gate dielectric which increases capacitance equivalent thickness. Molybdenum material is used as a gate electrode instead of poly-Si which can avoid this problem. In nanoscale FinFET devices, the quantum effects, non-equilibrium conditions, and ballistic transport have an impact on their performances. The Non-Equilibrium Green's Function (NEGF) model allows full quantum mechanical simulation of ballistic transport in nanoscale FinFET devices (Dastjerdy et al. 2011). As the silicon body cross-section is uniform for the device, the uncoupled mode space approach where NEGF formalism is in the transport direction is coupled with the Schrodinger equation in the transverse plane to find eigen energies and eigenfunctions that are considered for numerical simulation.

The effective mass approximation will reduce the computational complexity for the calculation of electron densities. The electron concentration is computed by solving the two-dimensional (2D) Schrodinger equation for each sub-band propagating from source to drain by providing the eigen parameter with the effective mass approximation along Z-direction, assuming that confinement is in the transversal X–Y plane.

5.3 Stability Modeling

The stability factor, K, indicates whether a device is conditionally/unconditionally stable. FinFETs are said to be unconditionally stable at any operating frequency above a critical frequency (f_k). Unconditionally stable means that the transistor will not begin to oscillate independently from the value of the signal source and load impedances from any additional passive termination networks at the transistor's input (gate terminal) and output (drain terminal). At operating frequency below

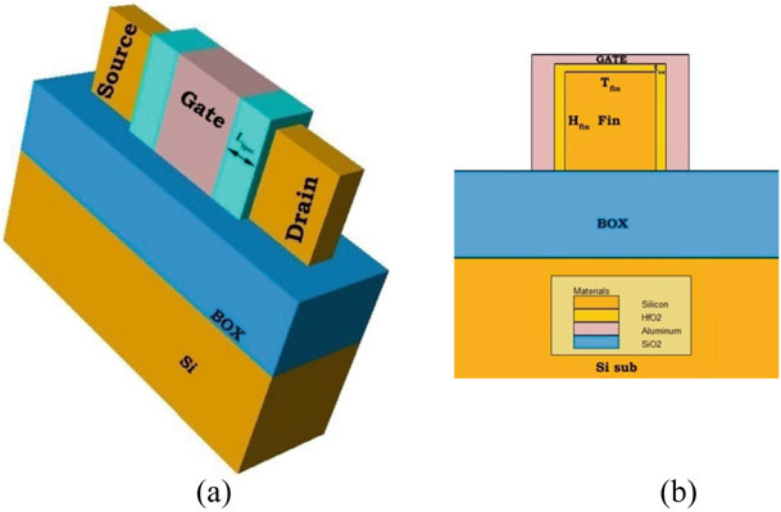

Fig. 5.1 **a** 3D schematic view of FinFET. **b** Cross-section view of FinFET showing T_{fin}, H_{fin}, t_{ox}, silicon substrate, and buried oxide (BOX)

f_k, however, the transistor is conditionally stable and certain termination conditions can cause oscillation. Hence, the device must satisfy the condition $K > 1$ to be unconditionally stable.

The stability factor can be calculated using Y-parameters at different frequencies of operation for FinFET. The stability factor in terms of Y-parameters can be expressed as

$$K = \frac{2R_e(Y_{11})R_e(Y_{22}) - R_e(Y_{12}Y_{21})}{|Y_{12}.Y_{21}|} \tag{5.1}$$

The Y-parameters which include all of the small-signal parameters that dominate device behavior of SOI-FinFET can be expressed as, In Kang et al. (2006),

$$Y_{11} = \omega^2\left(R_{gd}C_{gd}^2 + R_{gs}C_{gs}^2\right) + j\omega\left(C_{gd} + C_{gs}\right) \tag{5.2}$$

$$Y_{12} = -\omega^2 R_{gd}C_{gd}^2 - j\omega C_{gd} \tag{5.3}$$

$$Y_{21} = g_m - \omega^2 R_{gd}C_{gd}^2 - j\omega\left(C_{gd} + g_m\tau_m\right) \tag{5.4}$$

$$Y_{22} = g_{ds} + \omega^2 R_{gd}C_{gd}^2 + j\omega\left(C_{sdx} + C_{gd} - L_{sd}g_{ds}^2\right) \tag{5.5}$$

These Y-parameters can be used in Eq. (5.1) to simplify further as

$$K = \frac{\left[\omega^2 A + \omega^4 B\right]^2}{\left[\omega^4 C - \omega^2 D\right]^2 + \left[\omega^3 E - \omega F\right]^2} \tag{5.6}$$

where

$$\begin{aligned}
A &= R_{gd} C_{gd}^2 g_{ds} + R_{gs} C_{gs}^2 g_{ds} - R_{gd} C_{gd}^2 g_m - C_{gd}^2 + C_{gd} g_m \tau_m, \\
B &= R_{gd} C_{gd}^2 + R_{gd}^2 C_{gd}^4, \\
C &= R_{gd}^2 C_{gd}^4, \\
D &= R_{gd} C_{gd}^2 g_m + C_{gd}^2 + C_{gd} g_m \tau_m, \\
E &= R_{gd} C_{gd}^3 + g_m \tau_m R_{gd} C_{gd}^2, \\
F &= g_m C_{gd},
\end{aligned}$$

C_{gs} is total gate to source, C_{gd} is total gate to drain, C_{gg} is total gate capacitance $\left(C_{\mathrm{gg}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}\right)$, g_m is transconductance, g_{ds} drain to source conductance, R_{gs} is gate to source resistance, and R_{gd} is gate to drain resistance.

Substituting $K = 1$ and solving Eq. (5.6) by considering the approximation $\omega^2 R_{\mathrm{gd}}^2 C_{\mathrm{gd}}^2 \ll 1$, $\omega^2 R_{\mathrm{gs}}^2 C_{\mathrm{gs}}^2 \ll 1$, $\omega^2 g_{\mathrm{ds}}^2 L_{\mathrm{sd}}^2 \ll 1$ and $\omega^2 \tau_m^2 \ll 1$, we obtain f_k as

$$f_k \cong \frac{f_t}{N\sqrt{g_m(R_{\mathrm{gs}}^2 + R_{\mathrm{gd}}^2)M + NM(g_{\mathrm{ds}} R_{\mathrm{gs}} + g_m R_{\mathrm{gd}} + 1)}} \tag{5.7}$$

where $M = \frac{C_{\mathrm{gs}}}{C_{\mathrm{gg}}}$, $N = \frac{C_{\mathrm{gd}}}{C_{\mathrm{gg}}}$, and $f_t = \frac{g_m}{2\pi C_{\mathrm{gg}}}$

The total (intrinsic + extrinsic) gate to source (C_{gs}) and gate to drain (C_{gd}) capacitances Angsuman Sarkar (2012) without considering overlap capacitance can be calculated as

$$C_{\mathrm{gs}} = C_{\mathrm{gsi}} + C_{\mathrm{fext}} + C_{\mathrm{fint}} \tag{5.8}$$

$$C_{\mathrm{gd}} = C_{\mathrm{gdi}} + C_{\mathrm{fext}} + C_{\mathrm{fint}} \tag{5.9}$$

The internal and external fringing capacitances can be expressed as Enz et al. (2006)

$$\begin{aligned}
C_{\mathrm{fint}} = &\left[\frac{W\varepsilon_{\mathrm{si}}}{3\pi}\ln\left(1 + \frac{t_{\mathrm{si}}}{2t_{\mathrm{ox}}}\sin\left(\frac{\pi}{2}\frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{si}}}\right)\right)\right] \\
&\times \mathrm{e}^{-\left((V_{\mathrm{gs}} - V_{\mathrm{FB}} - 2\phi_f - V_{\mathrm{ds}})/(3/2)\Phi_f\right)^2}
\end{aligned} \tag{5.10}$$

$$C_{\mathrm{fext}} = \left[\frac{2W\varepsilon_{\mathrm{ox}}}{3\pi}\ln\left(1 + \frac{t_{\mathrm{g}}}{t_{\mathrm{ox}}}\right)\right] C_{\mathrm{fext}} = \left[\frac{2W\varepsilon_{\mathrm{ox}}}{3\pi}\ln\left(1 + \frac{t_{\mathrm{g}}}{t_{\mathrm{ox}}}\right)\right] \tag{5.11}$$

where ε_{si} and ε_{ox} are dielectric constants of silicon and oxide materials; W, t_{si}, t_g, and t_{ox} are the width, thickness of silicon body, gate contact, and gate oxide, respectively. V_{FB} and ϕ_f are the flat band voltage and Fermi potential, respectively.

Equation (5.7) describes the relation between critical frequency, intrinsic small-signal parameters, and cut-off frequency (f_t) which help to optimize the device. It is evident from Eq. (5.7) that M and N values can be adjusted to decrease f_k without f_t degradation. The optimization of the FinFET structure lies in the study of factors related to M and N, especially C_{gs} and C_{gd}. Equations (5.8–5.11) show the bias and geometry dependence on C_{gs} and C_{gd} of FinFET. By adjusting the applied gate bias, drain bias, and geometrical parameters such as aspect ratio (AR), gate spacer length (L_{spac}), along with gate material work function (Φ_m), the FinFET can be optimized for improved stability performance.

5.4 Bias Optimization of FinFET: RF Stability Perspective

The effect of the gate to source and gate to drain bias on RF stability performance of FinFET is discussed in this section. It is evident from Eqs. 5.7–5.11 that the bias dependency of small-signal parameters has an impact on the cut-off frequency and maximum oscillation frequency.

5.4.1 Optimization of Gate to Source Voltage

The extracted stability factor for different gate to source voltage (V_{gs}) at drain to source voltage (V_{ds}) of 0.1 V is shown in Fig. 5.2. It is evident from Fig. 5.2 that for larger gate bias, FinFET reaches unconditional stability at an earlier frequency as compared to smaller gate bias. With further increase in V_{gs}, C_{gs} gets saturated and affects the parasitic resistance which degrades the RF performance.

It is observed from Fig. 5.3 that at higher gate bias, f_k reaches 32 GHz as compared to smaller gate bias with f_k greater than 450 GHz. Hence, higher gate bias is preferred to operate the FinFET in the RF range.

5.4.2 Optimization of Drain to Source Voltage

The stability factor is calculated from extracted Y-parameters for various applied drain ($\mathrm{V_{ds}}$) biases with gate (V_{gs}) bias of 1.5 V which are shown in Fig. 5.4. It is evident from Fig. 5.4 that FinFET attains unconditionally stable condition at lower V_{ds} since C_{gs} dominates C_{gd} at higher drain bias.

Figure 5.5 shows the extracted critical frequency for various drain biases and fixed gate bias (V_{gs}) of 1.5 V. As V_{ds} increases, the stability performance degrades since

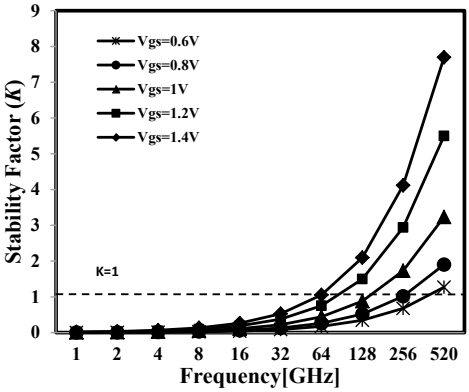

Fig. 5.2 Extracted stability factor for different V_{gs} at V_{ds} = 0.1 V

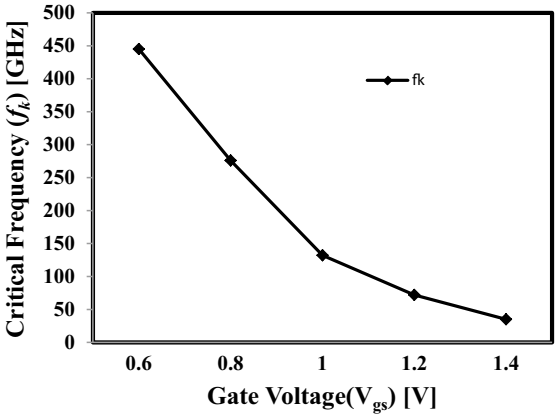

Fig. 5.3 Critical frequency as a function of gate voltage for $V_{ds} = 0.1$ V

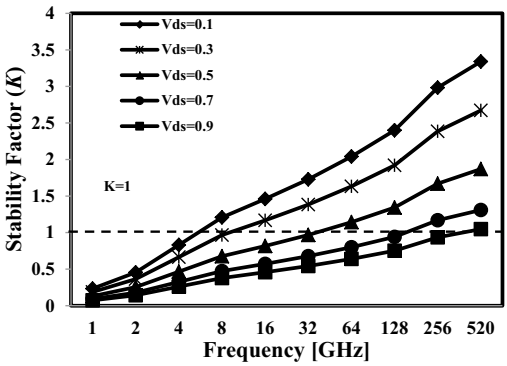

Fig. 5.4 Extracted stability factor for different V_{ds} at V_{gs} = 1.5 V

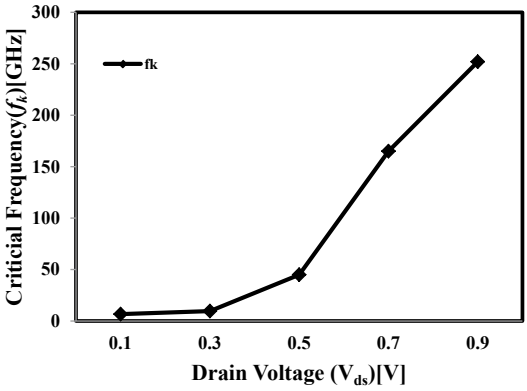

Fig. 5.5 Critical frequency as a function of drain voltage at $V_{gs} = 1.5$ V

Drain Induced Barrier Lowering (DIBL) affects the device performance at higher V_{ds} and degrades C_{gd}. It is observed from Fig. 5.5 that at lower drain bias, critical frequency reaches 6.5 GHz as compared to higher drain bias which is greater than 250 GHz. Hence, smaller drain bias is preferred to operate the FinFET in the RF range with better stability.

5.5 Geometry Optimization of FinFET: RF Stability Perspective

The FinFET geometrical parameters gate spacer length, fin height, and fin thickness influence its high-frequency performance. This section presents the optimization strategy of the geometrical parameters for improved high-frequency performance of FinFET.

5.5.1 Optimization of Gate Spacer Length

The stability factor, C_{gd}, and C_{gs} (inset) for different gate spacer lengths (L_{spac}) are shown in Fig. 5.6. The spacer length is given as the length of the spacer region covered on either sides of the silicon fin (source and drain region) adjacent to the gate. The gate spacer improves device subthreshold characteristics and reduces off current. The reduction in spacer length leads to an increase in short channel effects (SCEs) and has an impact on the RF stability performance of FinFET.

The fringing capacitance increases with smaller spacer length but causes oscillation at a higher frequency. The FinFET reaches stability at the critical frequency of 48 GHz for a spacer length of 10 nm as C_{gd} and C_{gs} increase with spacer length. The increase in spacer length shifts the source/drain doping away from the gate edge

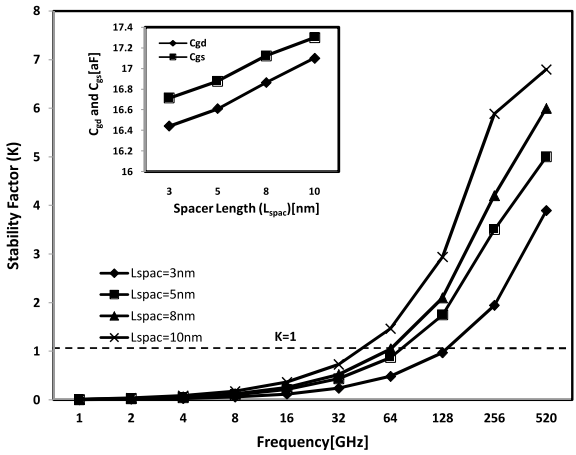

Fig. 5.6 Extracted stability factor, C_{gs}, and C_{gd} (inset) for different gate spacer lengths

resulting in reduced fringing capacitance. Further increase in spacer length will not affect stability because C_{gd} and C_{gs} saturate for larger spacer length, which is due to outer fringing capacitance decreasing exponentially with an increase in spacer length.

5.5.2 *Optimization of Fin Height and Fin Thickness*

Optimization of fin height and fin thickness plays an important role in optimizing the FinFET for RF applications. Figure 5.7 shows the extracted stability factor and C_{gd} (inset) for aspect ratio (AR) of three with four different fin heights (H_{fin}) and fin thickness (T_{fin}) values. The aspect ratio which is given as the ratio of H_{fin} to T_{fin} of three exhibits better RF performance Abhinav Kranti et al. (2008). For three different H_{fin} and T_{fin} values with AR $= 3$, the result shows better stability performance for T_{fin} of 8 nm and H_{fin} of 24 nm. FinFET has the advantage of varying silicon thickness in vertical plane, i.e., freedom of varying H_{fin} than T_{fin} to improve device performance. It can be observed that as H_{fin} increases, C_{gd} increases which leads to better stability performances. But a further increase in H_{fin} leads to an increase in aspect ratio which changes device architecture from quasi-triple gate to double gate. The FinFET reaches stability at the critical frequency of 14 GHz for fin thickness of 8 nm and fin height of 24 nm.

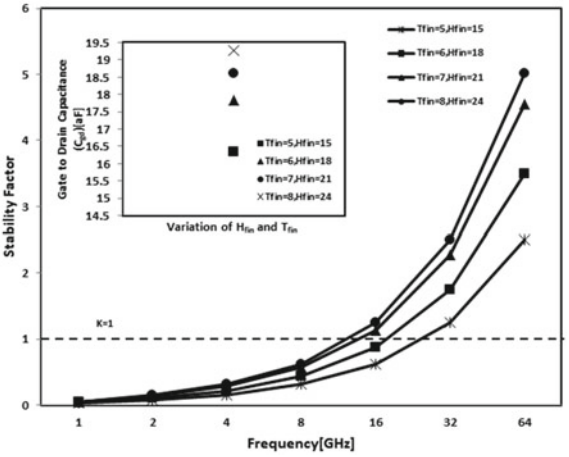

Fig. 5.7 Extracted stability factor and C_{gd} (inset) for different T_{fin} and H_{fin} with AR = 3

5.6 Optimization of Gate Work Function—RF Stability Perspective

The stability factor and C_{gd} (inset) for different gate metal work function (Φ_m) are shown in Fig. 5.8. Threshold voltage of FinFET device can be tuned by adjusting the work function of the gate material. The gate material work function can be varied based on gate material with nitrogen implantation dose and energy (Tawfik and Kursun 2008). Gate to drain capacitance increases at lower Φ_m due to capacitive coupling between the drain and gate electrodes. For gate metal work function of 4.5 eV, FinFET reaches stability at the critical frequency of 50 GHz as compared to higher gate metal work function. The gate to drain capacitance decreases with an increase in Φ_m which leads to an increase in f_k. Hence, smaller gate metal work function is preferred to operate FinFET under RF range.

5.7 Optimized FinFET Structure for Improved RF Stability Performance

It is observed that the proposed FinFET structure exhibits better stability performance at $H_{fin} = 24$ nm, $T_{fin} = 8$ nm, $\Phi_m = 4.5$ eV, and $L_{spac} = 10$ nm. Figure 5.9 shows the stability factor for the optimized bias and geometry FinFET structure.

The FinFET can be operated unconditionally stable at the critical frequency of 10 GHz. It indicates that FinFET does not require an additional stabilization circuit beyond 10 GHz onward for RF applications.

Figure 5.10 shows the cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) using the extracted intrinsic and extrinsic parameters as a function of drain current for the optimized FinFET. The bias and geometry optimized structure has

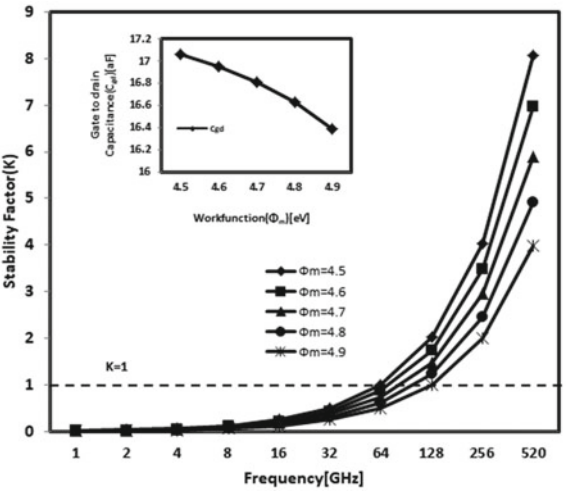

Fig. 5.8 Extracted stability factor and C_{gd} (inset) for a different gate work function

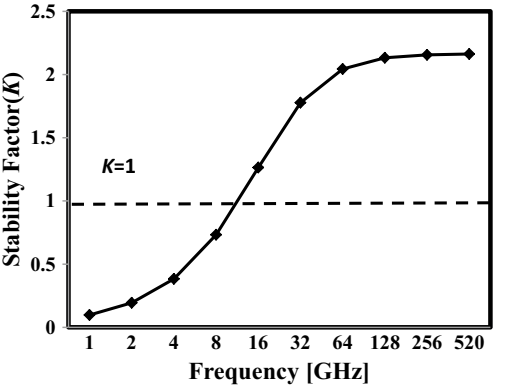

Fig. 5.9 Extracted stability factor for optimized FinFET at $V_{gs} = 1.5$ and $V_{ds} = 0.1$ V

maximum f_t of 675 GHz due to the improved g_m and f_{max} of 780 GHz, which shows that the proposed FinFET structure is suitable for high-frequency applications and can be operated with better stability from 10 GHz onward.

5.8 Summary

The RF stability performance of FinFET is extensively discussed at optimized bias and geometry conditions. The bias conditions such as gate bias and drain bias and geometrical parameters, such as gate spacer length and silicon body aspect ratio along with gate material work function are analyzed. It is observed that C_{gd} is responsible for degradation in critical frequency. The proposed device geometry and optimized

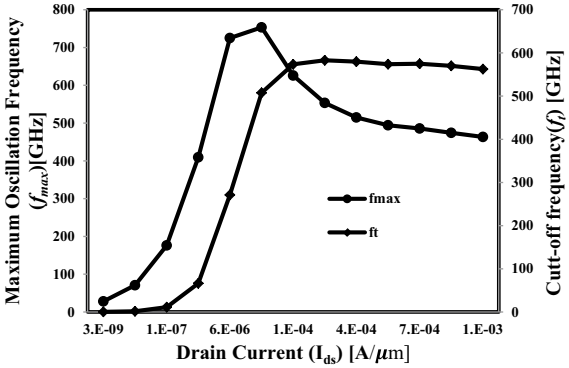

Fig. 5.10 f_t and $f_{\max}$ as a function of drain current for optimized FinFET at $V_{\mathrm{gs}} = 1.5$ V and $V_{\mathrm{ds}} = 0.1$ V

bias conditions show excellent RF stability performance. Hence, there is no additional circuit required for the proposed FinFET as the device is unconditionally stable from 10 GHz onward when operating in the RF range.

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Chapter 6
Radio Frequency Stability Performance of Silicon Nanowire Transistor

Abstract The structure and bias optimization techniques for the radio frequency (RF) stability of silicon nanowire transistor is presented. The RF parameters are extracted using device simulation. The device stability is obtained for various bias conditions and geometry. The impact of gate contact alignment and silicon radius on RF stability performance of Silicon Nanowire Transistor is presented and guidelines are provided for improved stability response.

Keywords Silicon nanowire transistors · Radio frequency · Stability factor · Device simulation

6.1 Introduction

The multigate structures of MOSFET are described in the previous chapters. It is found that the gate-all-around structure associated with a nanowire-shaped semiconductor offers the best possible electrostatic control of a channel. The gate-all-around structure becomes one of the promising solutions for the short channel device, with improved transport properties and better compatibility with Complementary Metal Oxide Semiconductor (CMOS) technologies. Silicon nanowire field-effect transistors (SNWTs) have attracted attention as promising devices due to their capability of ultrasensitive, selective, and real-time detection. Many investigations were reported on compact modeling, DC characteristics, and fabrication process of SNWT, Zhuge et al. (2008), Iniguez et al. (2006), Sato et al. (2009). In the design of radio frequency (RF) amplifiers or oscillators, the selection of transistors depends on their power gain, DC bias, noise, impedance matching, and stability. Many literatures were carried out to improve RF properties of non-planar MOS devices, such as DG MOSFETs, FinFETs, and SNWT. The RF parasitic optimization has been done to improve the maximum stable gain (MSG), maximum power gain, maximum oscillation frequency ($f_{\max}$), cut-off frequency (f_t), and reduced noise figure (NF), Wu et al. (2007), Parvais et al. (2007), Wang et al. (2007). In this chapter, the RF stability performance of silicon nanowire transistor (SNWT) is discussed for various bias conditions and geometries. The relation between stability factor and parasitic elements is derived using the intrinsic small-signal model and RF parameters.

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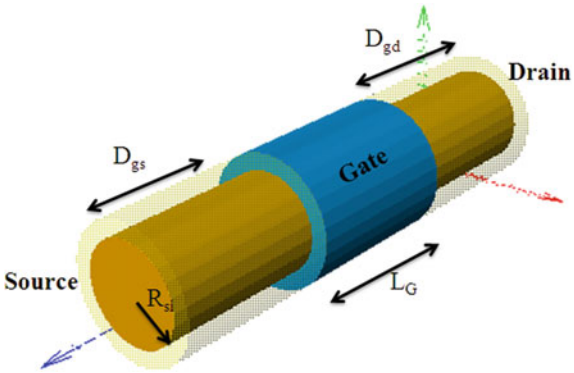

Fig. 6.1 Structure of silicon nanowire transistor

6.2 Numerical Modeling of Silicon Nanowire Transistor

The silicon nanowire transistor can be designed and modeled using a numerical simulator like Technology Computer Aided Design (TCAD) to analyze the electrical behavior of the device. Figure 6.1 shows the schematic structure of the silicon nanowire transistor. The radius of the silicon region (R_{si}) is 5 nm with an oxide thickness of 1 nm and the gate length (L_g) of 60 nm. Silicon dioxide (SiO_2) is used as gate dielectric material. The source and drain regions are doped uniformly at 2×10^{20} cm^{-3} and uniform channel doping of 1×10^{15} cm^{-3}. The distance between gate and source (D_{gs}) and between gate and drain (D_{gd}) is 20 nm. Density gradient (potential correction) quantum-corrected 3D drift–diffusion model coupled with Poisson's equation can be used to model the confinement of SNWT. After the model calibration, is applied to the AC device simulation of SNWTs to obtain intrinsic and extrinsic parameters.

6.3 Stability Modeling

The stability factor describes the unstable oscillations due to input or output impedance of the transistor which has a negative real part, the negative resistance yield $\Gamma_{in} > 1$ and $\Gamma_{out} 1 > 1$ (Pozar 1997). Therefore, the instability also depends on the input and output matching properties of the circuit. The transistor will be unconditionally stable if it has $\Gamma_{in} < 1$ and $\Gamma_{out} 1 < 1$ at a particular frequency. On the other hand, conditional stability determines the stable operation at a range of impedance values on the source or load matching. The conditions for unconditionally stable transistors are

$$|\Gamma_{in}| = \Gamma \left| S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \right| < 1 \tag{6.1}$$

$$|\Gamma_{\text{out}}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1 \tag{6.2}$$

Here, Γ_S and Γ_L are reflection coefficients at the source and load, respectively. A stability factor K was proposed with an auxiliary factor Δ to ensure these conditions

$$K = \left(\frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \right) \tag{6.3}$$

where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{6.4}$$

Here, S_{ij} (for $i, j = 1, 2$) are scattering parameters of the transistor.

A stability model can help to optimize the device geometry for RF active circuits. The stability model is developed based on the conditions mentioned in Eqs. (6.3) and (6.4). The stability factor in terms of Y-parameters is,

$$K = \frac{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12}Y_{21})}{|Y_{12} \cdot Y_{21}|} \tag{6.5}$$

The Y-parameters are considered with intrinsic small-signal parameters of SNWTs (Cho 2011),

$$Y_{11} \approx \omega^2 R_{\text{gd}} C_{\text{gd}}^2 + j\omega\left(C_{\text{gs}} + C_{\text{gd}}\right) \tag{6.6}$$

$$Y_{12} \approx -\omega^2 R_{\text{gd}} C_{\text{gd}}^2 + j\omega C_{\text{gd}} \tag{6.7}$$

$$Y_{21} \approx g_m - \omega^2 R_{\text{gd}} C_{\text{gd}}^2 - j\omega(C_{\text{gd}} + \tau \cdot g_m) \tag{6.8}$$

$$Y_{22} \approx g_{\text{ds}} + \omega^2 R_{\text{gd}} C_{\text{gd}}^2 + j\omega C_{\text{gd}} \tag{6.9}$$

These Y-parameters can be used in Eq. (6.5) to simplify further as

$$K \cong \frac{\omega(R_{gs}g_{ds}C_{gg}^2 + 2R_{gd}g_mC_{gg}C_{gd} + C_{gg}^2}{C_{gd}\sqrt{2\omega^2 g_m C_{gg}^2 + g_m^2}} \tag{6.10}$$

where $C_{gg} = C_{gs} + C_{gd}$

Equation (6.10) is extended to obtain critical frequency (f_{k}) by substituting $K = 1$,

$$f_k \cong \frac{g_m N}{2\pi C_{gg}\sqrt{g_{ds} g_m R_{gs} M^2 + NM\left(g_m R_{gd} + 1\right)}} \tag{6.11}$$

where $M = \frac{C_{gs}}{C_{gg}}$ and $N = \frac{C_{gd}}{C_{gg}}$

which can be related to f_t as,

$$f_k \cong \frac{f_t N}{\sqrt{g_{ds} g_m R_{gs} M^2 + NM\left(g_m R_{gd} + 1\right)}} \tag{6.12}$$

where $f_t \cong \frac{g_m}{2\pi C_{gg}}$

This stability model describes the relation between f_k, intrinsic small-signal parameters, and f_t which also gives hints for optimization. It is clear from Eq. (6.8) that M and N values can be adjusted to reduce f_k since f_t should not be degraded. But N is the almost independent parameter on the stability model concerning f_t. So the optimization begins with the study of factors related to M and N, especially gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), and gate capacitance (C_{gg}).

6.4 Bias Optimization of SNWT—RF Stability Perspective

Optimization of bias is an important factor and plays significant role on RF stability. The effect of the gate to source and gate to drain bias on RF stability performance of silicon nanowire transistor is explained in this section.

6.4.1 Optimization of Gate to Source Voltage

Figure 6.2 shows the variation of capacitance as a function of gate to source voltage for drain to source voltage (V_{ds}) of 1 V. It is observed that the C_{gs} increases with an increase in gate bias, and the total capacitance is contributed by C_{gs}. For further increase in gate bias, C_{gs} saturates. This provides a hint that by adjusting C_{gs} through the gate and drain biases, the RF stability of SNWT can be improved. At higher gate bias, C_{gs} dominates C_{gd}; hence, by varying drain bias and gate bias, desired capacitance can be achieved.

The stability factor is calculated from extracted small-signal parameters for various applied voltage and is shown in Fig. 6.3, which exhibits a critical frequency of 370 GHz for gate bias of 0.7 V and drain bias of 1.3 V. It is evident from Fig. 6.3, $f_k = 21$ GHz and $f_k = 45$ GHz for $V_{gs} = 1$ V and 1.3 V, respectively, at drain bias of 0.7 V. This shows the improved stability performance obtained at higher gate bias and lower drain bias.

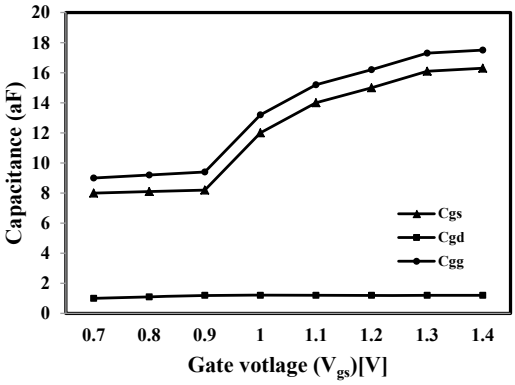

Fig. 6.2 Extracted capacitances for the sweep of V_{gs} for $V_{ds} = 1$ V

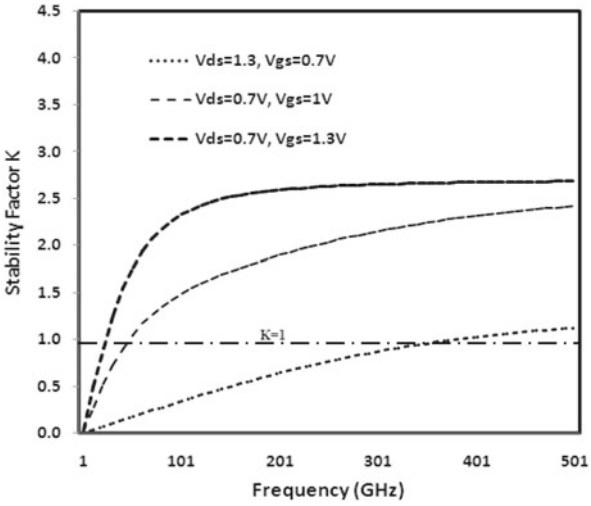

Fig. 6.3 Extracted stability factor at different bias conditions

6.4.2 Optimization of Drain to Source Voltage

Figure 6.4 shows the variations of C_{gs}, C_{gd}, and C_{gg} for different drain bias at a gate bias of 1 V. The variation of C_{gs} and C_{gd} is significant up to V_{ds} of 1 V. With a further increase in drain bias, capacitance decreases which degrades the stability performance. Figure 6.5 shows f_k and f_t as a function of frequency. At higher drain bias, C_{gd} dominates C_{gs} which leads to higher f_k. At higher drain bias, f_t increases as C_{gd} increases beyond it saturates. Hence, lower drain bias exhibits better stability performance.

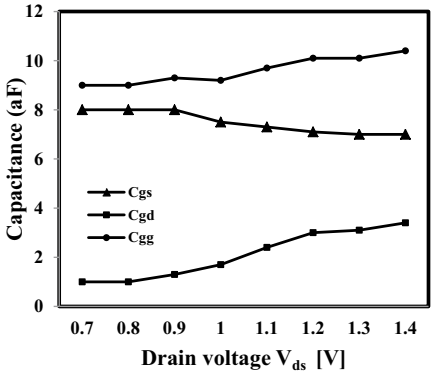

Fig. 6.4 Extracted capacitances for the sweep of V_{ds} and $V_{gs} = 0.7$ V

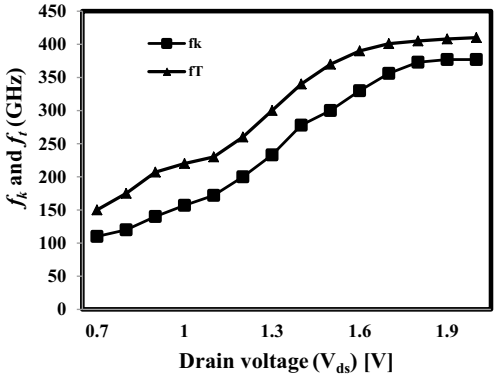

Fig. 6.5 Variation of f_k and f_t for the sweep of V_{ds}

6.5 Geometry Optimization of SNWT—RF Stability Perspective

The silicon nanowire transistor geometrical parameter such as gate contact alignment and silicon radius influences its high-frequency performance. This section presents the optimization strategy of the geometrical parameters for improved high-frequency performance of FinFET.

6.5.1 Optimization of Gate Contact Alignment

The position of the gate plays an important role to get higher C_{gs} and lower C_{gd}. The stability factor and C_{gs} are extracted for various D_{gs} and shown in Fig. 6.6. It is found that the stability has been improved as the gate moves toward the source because the gate overlap can cause variation in the fringing capacitance. The distance cannot be further reduced because of limitations during fabrication.

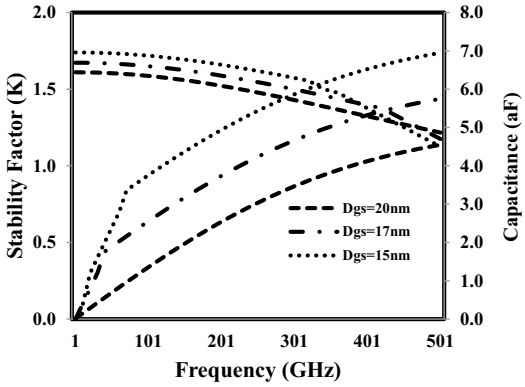

Fig. 6.6 Extracted stability factor and C_{gs} for different D_{gs} at $V_{gs} = 0.7$ V and $V_{ds} = 1.3$ V

6.5.2 *Optimization of Silicon Radius*

The silicon radius of the nanowire transistor plays an important role in device performance. Thinner radius leads to increased cut-off frequency due to higher g_m. Silicon radius thickness influences extrinsic parameters such as gate resistance, contact resistance, and parasitic capacitance. Stability factor K has been extracted for various radii of silicon nanowire and shown in Fig. 6.7. It is found that the stability degrades as the radius of silicon nanowire increases. This is due to the increase of g_m and f_t with silicon radius.

However, silicon radius can be optimized to achieve better critical frequency. From Fig. 6.7, it is evident that for silicon radius of 3 nm, device reaches unconditionally stable conditions at an earlier frequency.

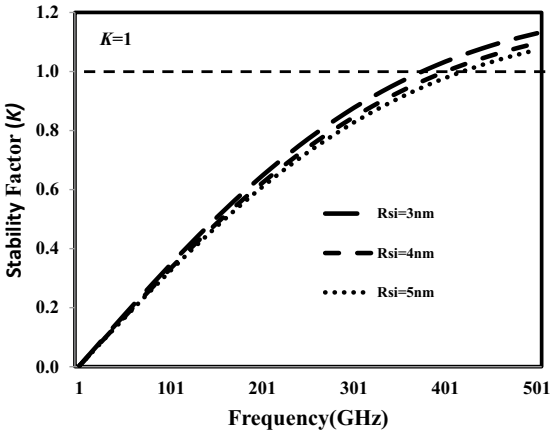

Fig. 6.7 Stability factor for various silicon radius

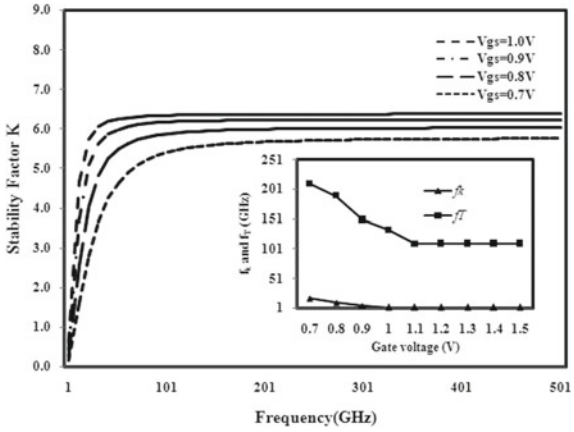

Fig. 6.8 Extracted stability factor for the optimized structure at different gate bias voltages and extracted f_t and f_k for the sweep of V_{gs} and $V_{ds} = 1$ V (inset)

6.6 Optimized SNWT for Improved RF Stability Performance

The optimized silicon nanowire transistor is discussed in this section based on the studies presented in the previous section. Figure 6.6 shows the extracted stability factor for various gate biases. It is observed that the stability response can be improved and $f_k = 29$ GHz at $V_{gs} = 1$ V. The f_k is extracted along with f_t at higher gate bias and is shown in the inset of Fig. 6.8. When $V_{gs} > 1$ V, the values of f_k and f_t are saturated; this indicates that the effect of capacitance at higher V_{gs} is negligible. The optimal geometry of the device has D_{gs} of 15 nm, t_{ox} of 1 nm, and R_{si} of 3 nm. For the optimal geometry and biasing conditions, the device shows unconditionally stable performance from 2 GHz onward with $f_t = 100$ GHz.

6.7 Summary

The RF characteristics of 60 nm SNWT can be studied through TCAD simulation. The device stability can also be studied for various biases and geometry conditions. The feedback capacitance C_{gd} from the drain to the gate is responsible for degradation in f_k and f_t. The optimized geometry and bias condition show excellent stability performance with optimal gain and f_t. There is no need for any additional stabilization network since the device is unconditionally stable from 2 GHz. The device shown in this chapter is of improved RF performance, reduced noise, and reduced circuit complexity. The optimized SNWTs can be a promising structure for mm-wave RFIC and Millimeter RF IC designs with reduced circuit complexity and noise level.

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Chapter 7
Radio Frequency Stability Performance of SELBOX Inverted-T Junctionless FET

Abstract In the recent times, the role of FinFET devices is increasing in the field of RF-IC design for realizing the high-frequency circuits. As a result, high-frequency characteristics including RF stability need to be investigated carefully. The impact of device geometrical and process parameter variations on the RF stability of 20 nm SELBOX inverted-T junctionless FinFET (SELBOX ITJLFET) is presented. The stability factor (K), critical frequency (fk), and its dependency on small-signal parameters (SSP) are investigated by varying the device and process parameters like gate work function (GWF), fin height (Hfin), fin width (Wfin), source underlap spacer length (LUS), and SELBOX length (LG). In addition, the relation between the bias and the stability factor of the device is also studied to identify the bias operating point in a RF stability perspective.

Keywords SELBOX · Inverted-T · Junctionless transistor · Process variation · RF stability · HfIn · Wfin

7.1 Introduction

The semiconductor sector has provided a roadmap for processing devices. The 22 nm node FinFET has already been approved by companies such as Intel and Taiwan Semiconductor Manufacturing Company (TSMC) (Bohr and Mistry 2011). Due to the high degree of confinement and the gap between the fins, FinFETs exhibit low leakage current (Zhang et al. 2006). To improve design efficiency or pitch current for a given area, the pitch between the fins has to be minimized (Mathew and Fossum 2008). To exploit the advantages of vertical and horizontal thin body structures, Mathew et al. and Zhang et al. fabricated a hybrid fin architecture known as inverted- "T" FET for the first time, which has overshadowed the performance of conventional FinFET (Mathew et al. 2005). Vandana et al. have further explored the impact of device geometry on the analog performance of inverted-T FinFETs at a 22 nm node with junctionless topology (Vandana et al. 2018). The buried oxide is patterned in the selective region under source and drain, and not continuously, which is referred to as the SELBOX structure. This chapter presents the analog and RF stability performance of Selective Buried Oxide (SELBOX) inverted-T junctionless FinFET with

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like different the gate work function, geometric parameters like fin width, fin height, and underlap spacer length. The design guidelines for better radio frequency stability performance are also discussed.

7.2 Virtual Fabrication Process Flow

The virtual fabrication process is a simulation-based method that supports engineers to define, simulate, and visualize the manufacturing process in a computer environment. By using virtual fabrication simulation tool such as Sentaurus Process, the manufacturing process can be defined and verified early in the design process. Sentaurus Process can be used for modeling of SELBOX ITJLFET. Figure 7.1 shows the process flow involved in the virtual fabrication of SELBOX ITJLFET, and the corresponding schematic view is portrayed in Fig. 7.2. In Sentaurus Process by specifying the 3D coordinates of specified length, the silicon substrate can be created. Then, selective oxidation using silicon dioxide (SiO_2) is performed to create Selective Buried Oxide (SELBOX) as shown in Fig. 7.2a. Subsequently, the epitaxial growth of silicon can be carried to have an inverted-T shaped fin, as shown in Fig. 7.2b. The Monte Carlo ion implantation process can be performed for a uniform doping profile in the fin area as shown in Fig. 7.2c. The deposition of Hafnium Oxide (HfO_2) can be carried out, which acts as gate oxide material as shown in Fig. 7.2d. After that, masking and etching of gate oxide need to be done for gate metal deposition. Figure 7.2e presents the schematic of the device after the deposition of spacer materials on both sides of the gate. Figure 7.2f presents the final device structure considered for simulation with source, drain, and gate contacts.

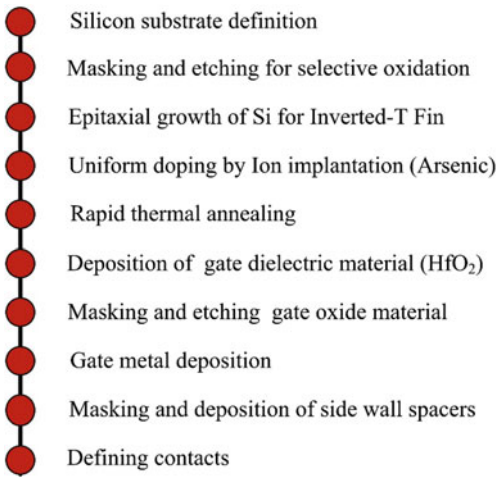

Fig. 7.1 Process flow for SELBOX ITJLFET

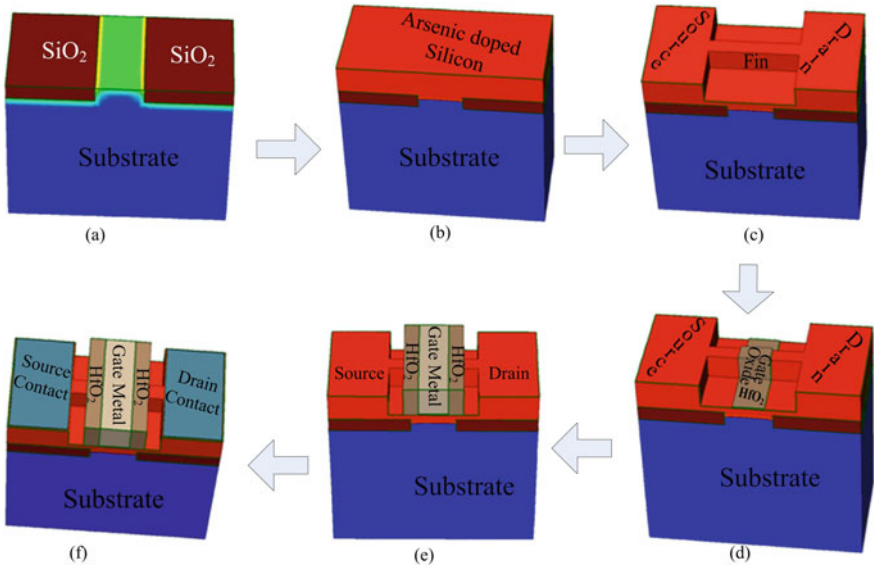

Fig. 7.2 Schematic of SELBOX ITJLFET for steps mentioned in Fig. 7.1

7.3 Numerical Modeling of SELBOX ITJLFET

The 3D schematic of the SELBOX ITJLFET along with high-k spacer material wrapped on both sides of the gate is shown in Fig. 7.3. The doping profile of the p-substrate of the device is maintained at 5×10^{18} cm^{-3}. To reduce the heating effects, a thin buried oxide (BOX) of SiO_2 layer of 10 nm thick is selectively created underneath source and drain areas through shallow trench isolation along with oxidation methods. Fin is uniformly doped with n-type impurity with a doping profile of 1×10^{-19} cm^{-3}. The gate oxide thickness of 0.9 nm is considered for HfO_2 dielectric material. To nullify the impact of the poly-gate depletion effect, a metal gate is used. Since the high-k spacers are directly in touch with Si fin, a virtual underlap is formed on both sides of the channel. The presence of this source underlap *(L_{US})* and drain underlap (L_{UD}) will, therefore, stimulate the fringing fields in the device and thereby improve the drive current. The device design parameters considered for the simulation are listed in Table 7.1.

The simulation models of SELBOX ITJLFET are calibrated with the experimental results of Paz et al. (2015). Figure 7.4 shows a close agreement between the simulation result and the experimental data. For device simulation, the drift–diffusion carrier transport model is enabled along with mobility degradation models like doping dependence for accounting scattering effects, high field saturation model for determining the high-k associated mobility degradation effects as well as velocity saturation effects, and transverse field for interfaces degradation effects. To quantify the impact of the recombination of holes and electrons, recombination models

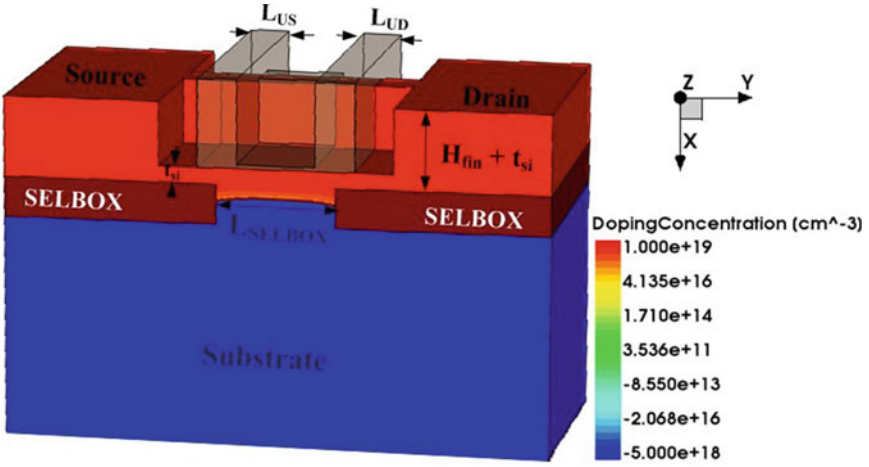

Fig. 7.3 3D schematic view of SELBOX ITJLFET

Table 7.1 SELBOX ITJLFET—design parameters

Parameters	Value/range
Gate length (L_g)	15–35 nm
UTB thickness (t_{si})	5 nm
Fin height (H_{fin})	10–40 nm
Fin width (W_{fin})	10–30 nm
BOX thickness	5 nm
Length of the SELBOX (L_{SELBOX})	10–40 nm
Gate work function (φ_{ms})	4.5–5 eV
Spacer length at source (L_{US}) and drain (L_{UD})	3–15 nm ($Hf\,O_2$)
Substrate doping (N_A)	5×10^{18} cm^{-3}
Device layer doping (N_D)	1×10^{19} cm^{-3}

such as Auger and Shockley Read Hall (SRH) can be integrated into the simulation. Band bending effects due to the high doping profile in the junctionless device can be considered by employing the old-Slotboom bandgap narrowing model. SRH model for temperature sensitivity and the thermodynamic model for carrier transport are also included. In addition, the quantum effects which arise in ultrathin body (UTB) layers and thin fins are taken into consideration by including a density-gradient quantum correction model.

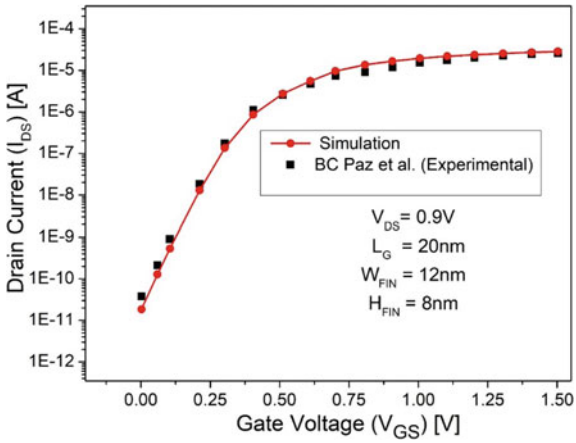

Fig. 7.4 Calibrated I_{DS}–V_{GS} characteristics of junctionless transistor topology with experimental data at $V_{DS} = 0.9$ V

7.4 Stability Modeling

Stability is one of the most important Figures of Merit (FoM) in the RF amplifier design perspective. So designing the amplifier should be in such a way that it has to be fabricated with absolute stability in the specified frequency. The complexity involved with RF stability at the circuit level can be reduced by identifying the potential stability (which could potentially oscillate) of the transistor at the device level itself. This can be accomplished by measuring the device's stability using the Stern stability model, which states that the device is unconditionally or conditionally stable (Rollett 1962). This model uses the stability factor (K) to test device stability, and if the value of K > 1 indicates that the transistor is unconditionally stable, otherwise it is conditionally stable and causes oscillations at a certain frequency.

In this section, the SELBOX ITJLFET is considered a two-port network with the gate as the input node and the drain as the output node. Then, the device is simulated for a range of frequencies to calculate the stability factor. The stability factor given by *P*. Stern in terms of Y-parameters is used to determine a transistor *K* value which is shown in Eq. 7.1 (Rollett 1962).

$$K = \frac{2Re(Y_{11})(Y_{22}) - Re(Y_{12})(Y_{21})}{|Y_{21}Y_{12}|} \tag{7.1}$$

where Y_{11} and Y_{22} are admittances at port 1 and port 2 and Y_{12} and Y_{21} are transfer admittances. The stability factor mentioned in Eq. 7.1 is further represented in terms of small-signal parameters after second-order frequency approximation and is given by Eq. 7.1 (Su et al. 2002)

$$K \cong \frac{\omega(2R_{gs}g_{ds}C_{gg}^2 + 2r_i g_{ds}C_{gg}^2 + 2R_g g_m C_{gd}C_{gg}^2 + C_{gd}^2)}{[\omega^2\left(C_{gd}^2 + 2R_g g_m C_{gd}C_{gg}^2\right)^2 + g_m^2 C_{gd}^2]^{1/2}} \tag{7.2}$$

Further simplification reduced to

$$K \cong \frac{(2R_{gs}g_{ds}C_{gg}^2 + 2r_i g_{ds}C_{gs}^2 + 2R_g g_m C_{gd}C_{gg}^2 + C_{gd}^2)}{\left[\left(C_{gd}^2 + 2R_g g_m C_{gd}C_{gg}^2\right) + \left(\frac{g_m C_{gd}}{\omega}\right)^2\right]^{1/2}} \tag{7.3}$$

$$K \cong \frac{\omega(2R_{gs}g_{ds}C_{gg}^2 + 2R_{gd}g_m C_{gd}C_{gg} + C_{gd}^2)}{C_{gd}\left(\sqrt{2\omega^2 g_m C_{gg}^2 + g_m^2}\right)} \tag{7.4}$$

The equation is further simplified to Eq. 7.4 by taking C_{gg} common

$$K \cong \frac{\omega C_{gg}\left(R_{gs}g_{ds} + 2R_{gd}g_m\left(C_{gd}/C_{gg}\right) + 1\right)}{C_{gd}\left(\sqrt{2\omega^2 g_m + \left(\frac{g_m}{C_{gg}}\right)^2}\right)} \tag{7.5}$$

By substituting $K = 1$ in Eq. 7.5, the critical frequency of the device can be deduced as shown in Eq. 7.6

$$f_k = \frac{f_t N}{\sqrt{\left(g_{ds}g_m R_{gs}M^2\right) + NM\left(g_m R_{gd} + 1\right)}} \tag{7.6}$$

where

$$M = \frac{C_{gs}}{C_{gg}} \tag{7.7}$$

$$N = \frac{C_{gd}}{C_{gg}} \tag{7.8}$$

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{7.9}$$

Another important RF performance parameter of the device is the critical frequency (f_k), which specifies the frequency, at which the device attains a unity stability factor. It draws the boundary line between the potentially stable and unconditionally stable devices and is seen as the bandwidth of an unstable transistor. The f_k of the device is calculated using Eq. 7.6 in terms of various device parameters (Su et al. 2002). Unity gain cut-off frequency (f_t) is one of the RF figures of merit, which gives the frequency at which transistor gain falls to unity is given in Eq. 7.9 in terms of small-signal parameters. The other parameters involved in Eq. 7.6 are: g_{ds} is output conductance, R_{gs} is the gate to source resistance, and C_{gg} is total gate capacitance. The total gate to source capacitance (C_{gs}) and total gate to drain capacitance (C_{gd}) without considering overlap capacitance are reported in Sarkar et al. (2012).

7.5 Impact of the Geometrical Parameter Variation on the RF Stability Performance

Normally, the stability factor (K) should be greater than one for any transistor to be unconditionally stable. However, it is decreasing with the decrease of frequency and further falls below 1 at low frequencies (Su et al. 2002) (no longer the device is unconditionally stable). So, therefore, our focus in this section is on improving stability in the low-frequency regime and reducing the potentially unstable bandwidth of the device.

7.5.1 Impact of Supply Voltages

Figure 7.5 shows the variation of stability factor against the frequency for different gate biases, while drain bias is fixed at 0.7 V. From Fig. 7.5, it is found that the critical frequency f_k is lowered with the increase in gate bias. Consider Eq. 7.6, the parameters R_g and g_{ds} are almost constant with V_{GS} and will not affect f_k, but the transconductance (g_m) and gate capacitance (C_{gg}) are V_{GS} dependent which impacts f_k. The C_{gg} (stronger gate bias dependent) increases with V_{GS}, whereas g_m decreases when V_{GS} is increased beyond 0.7 V, and due to the domination of C_{gg} over g_m, the stability factor and f_k are improving with the increase in V_{GS} (since the maximum g_m is obtained at $V_{GS} = 0.7$ V).

Figure 7.6 shows the variation of stability factor against the frequency for different drain biases, while gate bias is fixed at 1 V. A similar analysis can be made for identifying the impact of V_{DS} on stability and f_k. It is observed from Eq. 7.6 that

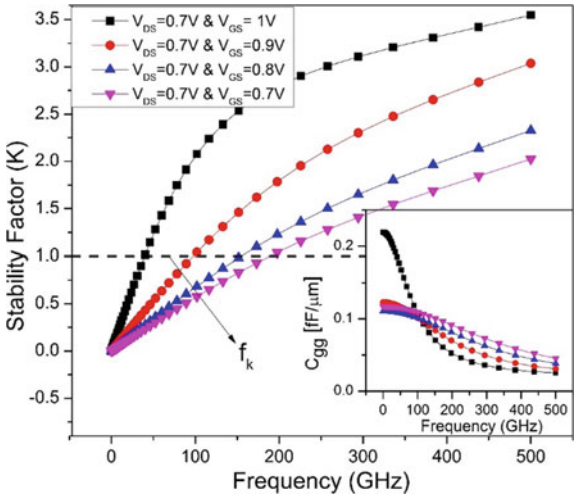

Fig. 7.5 Stability factor (K) and (inset) C_{gg} as a function of frequency for different V_{GS}

R_g remains constant with V_{DS} since it is not a drain bias dependent, whereas g_m, g_{ds}, and C_{gg} are V_{DS} dependent, with the former one marginally increasing and the latter two are decreasing with an increase in V_{DS}. The denominator of Eq. 7.6 has a stronger dependence on V_{DS} when compared to the numerator; therefore, the f_k of the device is increasing with the increase in drain bias. The small signal and RF parameter variation with V_{GS} and V_{DS} are presented in Tables 7.2 and 7.3.

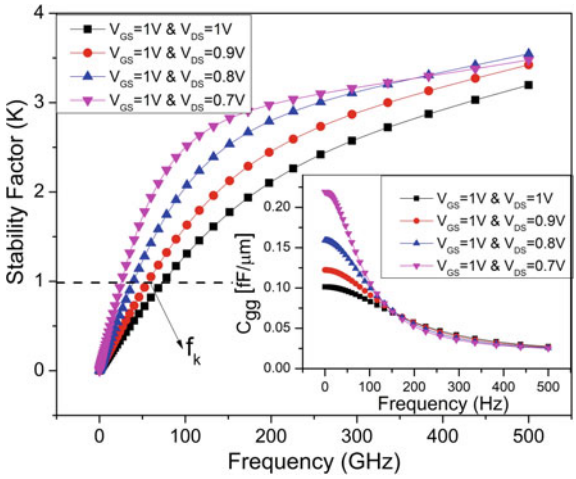

Fig. 7.6 Stability factor (K) and (inset) C_{gg} as a function of frequency for different V_{DS}

Table 7.2 Small signal and RF parameter variation for different V_{DS}

V_{DS} ($V_{GS} = 1$ V)	g_m (μS)	C_{gg} (fF)	f_t (GHz)	f_k (GHz)
0.7 V	47.2	0.22	34.3	27
0.8 V	51.2	0.16	51.3	40
0.9 V	53.3	0.12	69.4	59
1 V	54.3	0.1	85.3	78

Table 7.3 Small signal and RF parameter variation for different V_{GS}

V_{GS} ($V_{DS} = 0.7$ V)	g_m (μS)	C_{gg} (fF)	f_t (GHz)	f_k (GHz)
0.7 V	98.2	0.12	134.3	197
0.8 V	91.2	0.11	132	173
0.9 V	69.4	0.13	90	101
1 V	47.2	0.21	34.3	40

7.5.2 *Impact of Gate Length* (L_G)

Figure 7.7 shows the dependency of g_m and g_d on gate length (L_G) variation for a gate to source voltage (V_{GS}) varied from 0 to 1 V and drain to source voltage (V_{DS}) kept at 0.7 V. As L_G is scaled down from 35 to 15 nm, the device I_{ON} tends to increase due to increased electrostatic control of the gate over the channel; consequently, higher g_m is achieved at lower gate length. As with the scaling of L_G, the effective area of the channel gets reduced, thereby reducing the total gate capacitance C_{gg} of the device; this can be observed from Fig. 7.8 inset. Figure 7.8 shows the variation of f_t with L_G. From Eq. 7.9, the gate capacitance and transconductance have an opposite influence on f_t, hence the increment of g_m and degradation of C_{gg} resulting in an increase of f_t with the scaling of L_G.

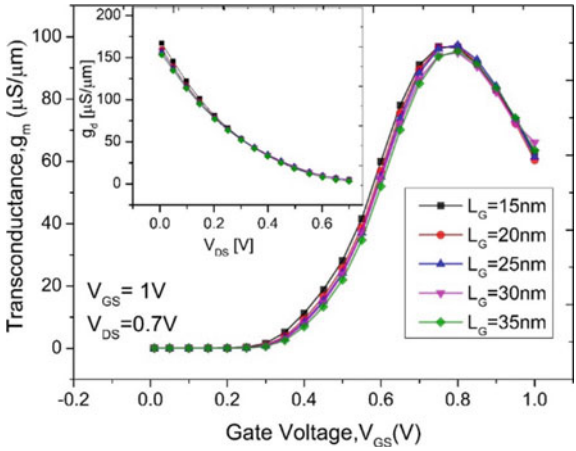

Fig. 7.7 g_m as a function of V_{GS} for different L_G and (inset) g_d as a function of V_{DS} for different L_G

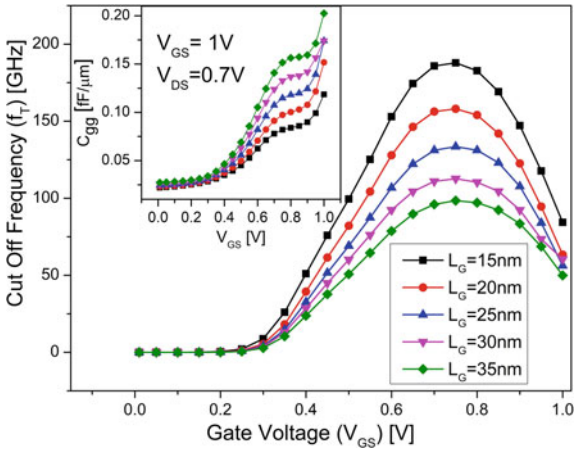

Fig. 7.8 f_t and (inset) C_{gg} as a function of V_{GS} for different L_G

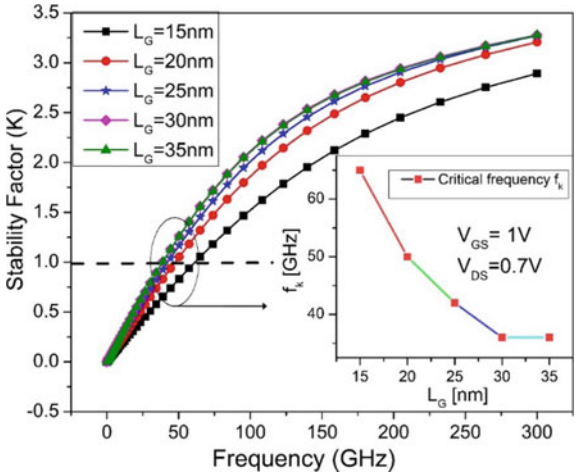

Fig. 7.9 Variation of stability factor (K) with frequency for different L_G and (inset) f_k as a function of L_G

Figure 7.9 shows the RF stability factor (K) with the frequency for different gate lengths of the SELBOX ITJLFET. As the gate length is increasing, the stability of the device is increasing, and thereby, the device is becoming unconditional stable at the lower frequency since it is dominated by the g_m and C_{gd} in the low-frequency region. The channel charging resistance $r_i C_{gs}$ would also increase the stability factor as observed in Eq. 7.2. Since $r_i C_{gs}$ is large for longer channel devices, therefore the device with a longer channel has a higher stability factor. The inset of Fig. 7.9 shows the critical frequency variation against the L_G. As the L_G is increasing from 15 to 35 nm, the f_k of the device is lowered. Since f_k is directly proportional to f_t, which falls as channel length is increased, thereby reducing the potentially unstable bandwidth from 65 to 32 GHz and making the device used in a wide range of frequency applications.

7.5.3 *Impact of SELBOX Length* (L_{SELBOX})

L_{SELBOX} represents the length between both the edges of the BOX material shown in Fig. 7.3. Figure 7.10 shows the g_m and g_{ds} variation (inset) with V_{GS} for different SELBOX lengths. For shorter SELBOX lengths, the device exhibits better g_m than longer SELBOX lengths, whereas drain conductance remains almost constant.

As with the increasing of L_{SELBOX}, the depletion region penetrates more into the active region thereby decreasing the ON current and impacting the g_m of the device.

Figure 7.11 shows the variation of cut-off frequency and C_{gg} with gate voltage for different SELBOX lengths. It is observed from Fig. 7.11 that C_{gg} is increasing with the increase of L_{SELBOX}. The decrease of g_m and increase of C_{gg} result in a decrease of f_t with the increase of L_{SELBOX}. Figure 7.12 shows the variation stability factor for different SELBOX lengths. From Fig. 7.12, it is evident that the device with a larger

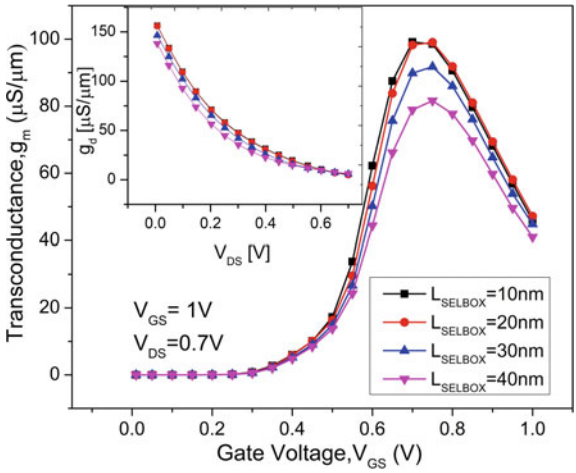

Fig. 7.10 g_m as a function of V_{GS} and (inset) g_d as a function of V_{DS} for different L_{SELBOX}

SELBOX length is attaining unconditional stability at a lower frequency and having higher stability when compared to a smaller SELBOX length. Referring to Eq. 7.5, it is known that the stability factor majorly depends on the small-signal parameters g_m, C_{gd}. With the increase in L_{SELBOX}, the transconductance is decreasing and gate capacitance is increasing, due to which the critical frequency f_k is decreasing, as shown in the inset of Fig. 7.12. The f_k is fallen from 27.2 GHz to 15.2 GHz when L_{SELBOX} is raised from 10 to 40 nm. All the quantitative values of small signal and RF parameters variation for different L_{SELBOX} are tabulated in Table 7.4.

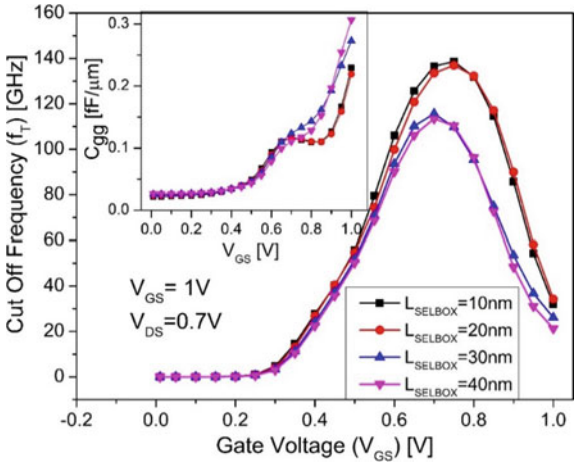

Fig. 7.11 f_t and (inset) C_{gg} as a function of V_{GS} for different L_{SELBOX}

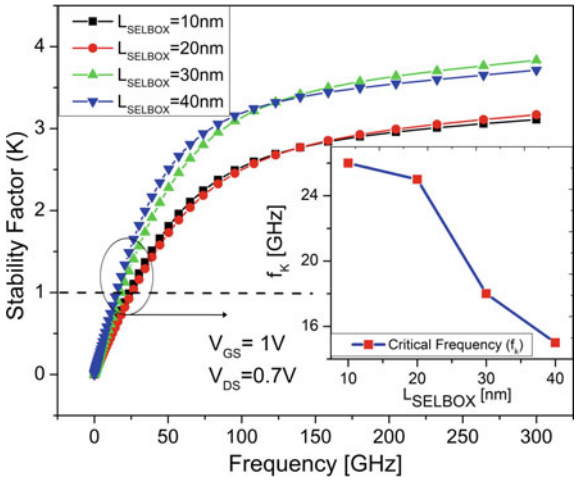

Fig. 7.12 Stability factor (K) as a function of frequency for different L_{SELBOX} and (inset) f_k as a function of L_{SELBOX}

Table 7.4 Small-signal model and RF parameter variation with L_{SELBOX}

L_{SELBOX}	g_m (μS)	C_{gg} (fF)	f_t (GHz)	g_d (μS)	C_{gs}/C_{gg}	C_{gd}/C_{gg}	f_k (GHz)
10 nm	99.2	0.229	137	5.23	0.655	0.34	27.2
20 nm	99	0.232	134	4.76	0.67	0.33	25
30 nm	91.8	0.273	116	5.97	0.71	0.029	20.6
40 nm	81.6	0.306	113	7.31	0.713	0.28	15.2

7.5.4 *Impact of Source Underlap Length* ($\mathbf{L_{US}}$)

The variation of g_m, C_{gg}, and f_t with V_{GS} for different lengths of source underlap (L_{US}) is shown in Fig. 7.13. For simulation, the L_{US} is varied from 3 to 15 nm by keeping L_{UD} at 10 nm. From Fig. 7.13, it is observed that g_m is slightly increasing with the increase of L_{US}. It is evident from Eq. 7.10 (Vandana et al. 2018) that g_m is directly proportional to the difference in charge at drain/source regions. This difference in charge is enhanced at gate edges by the increase of L_{US}. From Fig. 7.13 inset, it is observed that the gate capacitance is increasing with the increase of L_{US}. The increase in L_{US} offers a longer effective channel length, which increases the lateral extension of source depletion width, ultimately enhancing the outer fringing fields and thereby increasing the C_{gg}. Figure 7.13 shows the variation of f_t with L_{US}. As L_{US} increases, the f_t of the device is falling, since it is dominated by the increase of C_{gg} than the g_m.

$$g_m = \frac{\mu W}{L_{eff}}(Q_s - Q_d) \tag{7.10}$$

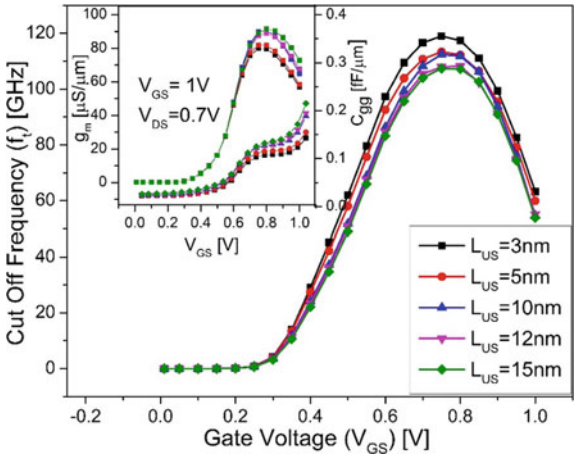

Fig. 7.13 f_t as a function of V_{GS} and (inset) g_m, C_{gg} as a function of V_{GS} for different L_{US}

Table 7.5 Small-signal model and RF parameter variation with L_{US}

L_{US}	g_m (μ S)	C_{gg} (fF)	f_t (GHz)	g_d (μS)	C_{gs}/C_{gg}	C_{gd}/C_{gg}	f_k (GHz)
3 nm	80	0.143	119	1.67	0.75	0.23	57
5 nm	81.8	0.155	113.4	1.79	0.75	0.22	52
10 nm	90.5	0.189	111.8	2.34	0.75	0.021	46
12 nm	91	0.195	108.1	2.35	0.76	0.21	44.5
15 nm	91.5	0.215	107.4	2.68	0.77	0.20	44

Table 7.5 Small-signal model and RF parameter variation with L_{US}

Figure 7.14 presents the stability factor variation with frequency for different lengths of source underlap and the gate capacitance with the frequency. From Fig. 7.14, the stability of the device is improved with the increase of L_{US}. As L_{US} is increasing, the small-signal parameters g_m and C_{gg} are increasing with the latter one dominating the former. Due to this, the g_m/C_{gg} ratio is decreasing and thereby improving the stability factor. The f_k of the device which is given by Eq. 7.6 has a stronger dependence of C_{gg} in the denominator, due to which it has fallen nearly by 25% with an increase of L_{US}. All the quantitative values of small signal and RF parameters variation for different L_{US} are tabulated in Table 7.5.

7.5.5 *Impact of Fin Height* (H_{fin})

Figure 7.15 shows the g_m and g_d variation (inset) with gate voltage for different fin heights. With the increase of H_{fin}, parasitic resistance is reduced due to which the device delivers a much-improved driving current, thereby significantly enhancing

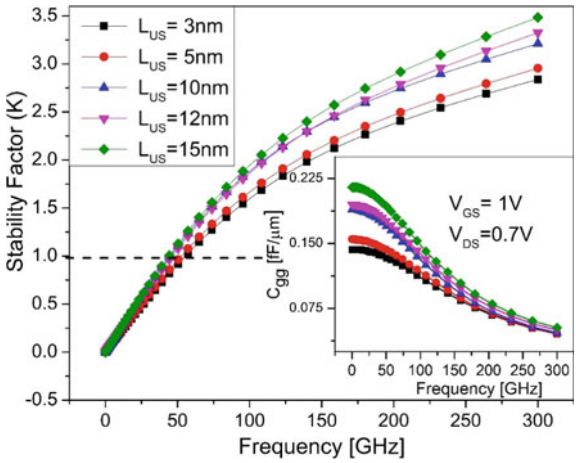

Fig. 7.14 Stability factor (K) as a function of frequency for different L_{US} and (inset) C_{gg} as a function of frequency for different L_{US}

the transconductance of the SELBOX ITJLFET. It is evident from Eq. 7.11 that the device with higher H_{fin} induces large fringing capacitance when compared to a smaller H_{fin} devices. This is due to the enhancement of the inner fields with the rise of H_{fin} and thereby increasing the gate capacitance, which is shown in the inset of Fig. 7.16. Both parameters g_m and C_{gg} are increased with fin height; as a result, f_t is increased marginally due to the dominance of g_m over C_{gg} as shown in Fig. 7.16.

$$C_{gg} = \frac{\in_{ox}}{T_{ox}}(2H_{\text{fin}} + W_{\text{fin}})L_g \tag{7.11}$$

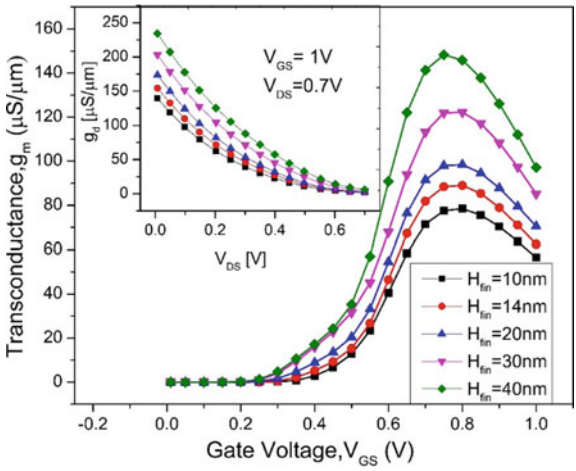

Fig. 7.15 g_m as a function of V_{GS} and (inset) g_{ds} as a function of V_{DS} for different H_{fin}

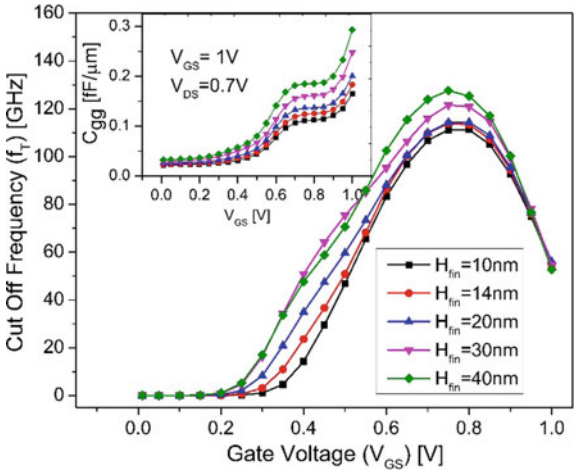

Fig. 7.16 f_t and (inset) C_{gg} as a function of V_{GS} for different H_{fin}

Figure 7.17 demonstrates that stability factor and critical frequency are not sensitive to the variation of fin height since the device is operated in saturation. As the fin height increases, the subsequent increase in C_{gg} is balanced simultaneously by the increase in g_m; as a result, a smaller variation in the stability factor and critical frequency is obtained. Moreover, it is not desirable to increase the fin height to a larger extent as there is a degree of freedom on varying H_{fin}. Since it attributes to the increase of off current of the device, it also affects the aspect ratio, due to which device structure changes from quasi-triple gate to a double-gate device. The lowest f_k of 40 GHz is achieved for H_{fin} of 40 nm. All the quantitative values of small-signal parameters and RF parameters variation with fin height are tabulated in Table 7.6.

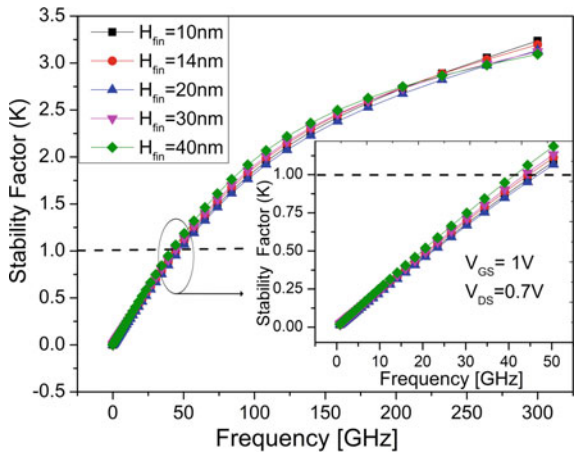

Fig. 7.17 Stability factor (K) as a function of frequency for different H_{fin}

Table 7.6 Small signal and RF parameter variation different H_{fin}

H_{fin}	g_m (μ S)	C_{gg} (fF)	f_t (GHz)	g_d (μS)	C_{gs}/C_{gg}	C_{gd}/C_{gg}	f_k (GHz)
10 nm	78.4	0.165	111.2	1.9	0.763	0.212	50
14 nm	88.9	0.183	113.8	2.34	0.748	0.22	46
20 nm	98.4	0.2	114.3	2.76	0.74	0.023	44.3
30 nm	122.7	0.247	121.5	4.3	0.72	0.26	42
40 nm	148.2	0.294	127.6	7.16	0.70	0.28	40

7.5.6 *Impact of Fin Width* (W_{fin})

The variation of g_m and g_{ds} with gate voltage for different fin widths is shown in Fig. 7.18, and it is observed that both of them are influenced by the variation of fin width. As fin width is scaled from 30 to 10 nm, the corresponding on current degrades due to the reduction of channel volume. A device with higher fin width has a larger g_m and gets half when fin width is scaled to 10 nm from 30 nm for a fixed fin height of 10 nm. As the g_m and C_{gg} are falling with the scaling of fin width, the combined effect of two parameters that has yielded the cut-off frequency, which is decreasing marginally and less sensitive to the scaling of fin width, is shown in Fig. 7.19.

Figure 7.20 shows the dependence of the stability factor on the frequency for different fin widths of SELBOX ITJLFET. From Fig. 7.20, it is evident that the stability of the device is improved with the scaling of fin width. As fin width is scaling, both small-signal parameters g_m and C_{gg} are decreasing, and the decrease of g_m is much higher than the reduction in C_{gg}, due to which the ratio of g_m/C_{gg} is reducing, thereby improving the stability factor. It is also noticed from Fig. 7.20 that

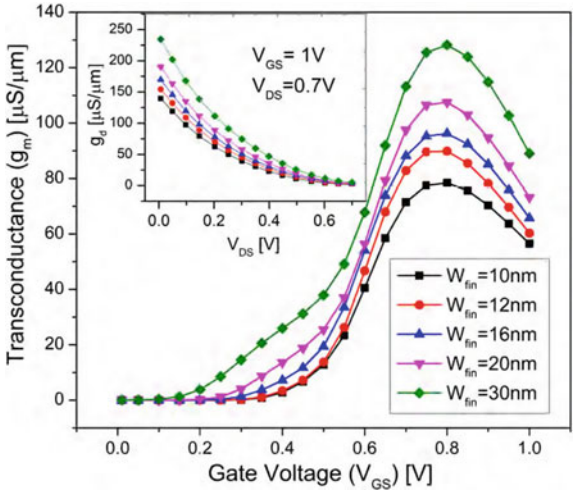

Fig. 7.18 g_m as a function of V_{GS} for different W_{fin} and (inset) gd as a function of V_{DS} for different W_{fin}

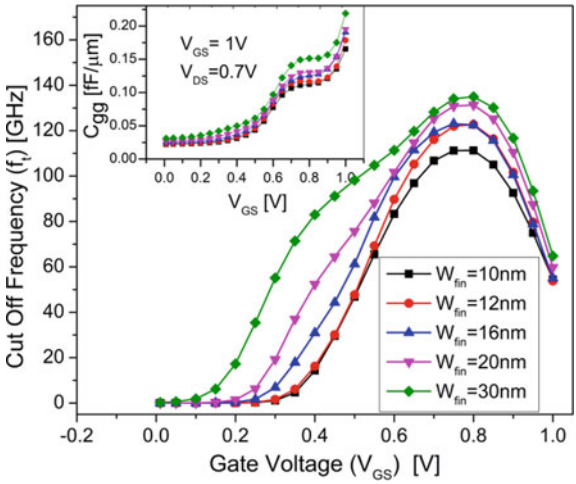

Fig. 7.19 f_t and (inset) C_{gg} as a function of V_{GS} for different W_{fin}

the device with smaller fin width has lower f_k and attains unconditionally stable at a lower frequency. This is mainly attributed due to the lower g_m and moderate gate capacitance associated with lower fin width.

The device with a fin width of 10 nm has an f_k of 45 GHz, whereas the 30 nm fin width device has an f_k of 55 GHz. All the quantitative values of small signal and RF parameters variation with fin width are tabulated in Table 7.7.

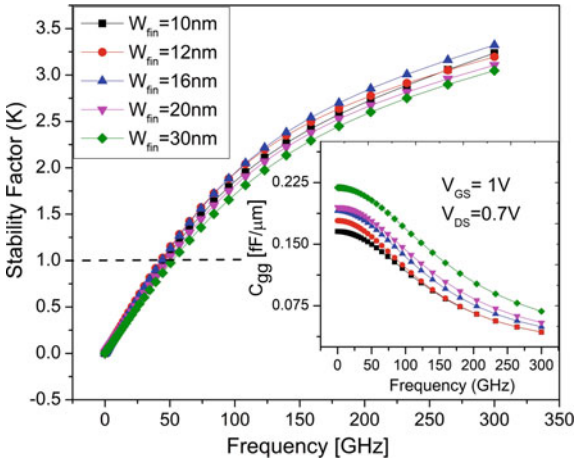

Fig. 7.20 Stability factor (K) and C_{gg} (inset) as a function of frequency for different $W_{\text{f in}}$

Table 7.7 Small signal and RF parameter variation for different W_{fin}

H_{fin} (nm)	g_m (μ S)	C_{gg} (fF)	f_t (GHz)	g_d (μ S)	C_{gs}/C_{gg}	C_{gd}/C_{gg}	f_k (GHz)
10	78.6	0.165	111.2	1.19	0.76	0.20	45
12	90.4	0.179	123	2.44	0.73	0.23	48
16	97.5	0.2	125	3.75	0.75	0.023	50
20	108	0.2	132	4.2	0.73	0.235	52
30	128	0.216	136	5.2	0.74	0.024	55

7.5.7 *Impact of Gate Work Function (φ_{ms})*

Figure 7.21 depicts the variation of g_m and g_d with the variation of the gate work function. From Fig. 7.21, it is observed that as the work function is increased from 4.5 to 5 eV, the transconductance of the device is unaffected and only maximum transconductance has been shifted from $0.5V_{GS}$ to V_{GS}. This is mainly due to a linear change in threshold voltage with an increase in gate work function. The gate capacitance C_{gg} in conventional devices is less significant to work function due to the presence of screening effects (Hwang et al. 2009). But in junctionless devices, the work function impacts C_{gg} significantly.

From Fig. 7.22 inset, it is seen that gate capacitance decreases with the increase of gate work function since the large gate work function completely depletes the channel. Figure 7.22 shows the variation of f_t with the work function. Since the variation of f_t is dominated by the large value $g_{m,\,\max}$ over the gate capacitance, therefore f_t of the device remains the same and unaffected by the variation of work function.

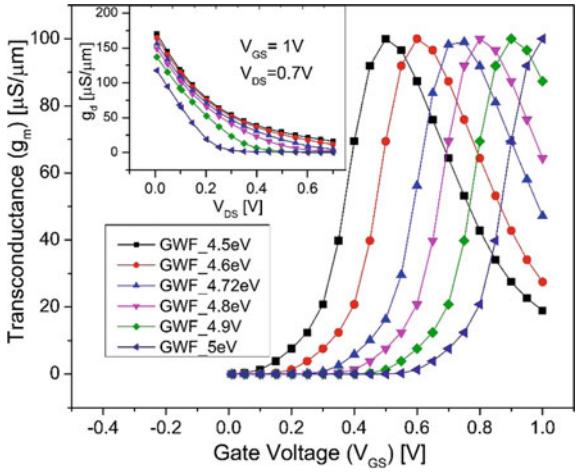

Fig. 7.21 g_m as a function of V_{GS} for different φ_{ms} and (inset) g_d as a function of V_{DS} for different φ_{ms}

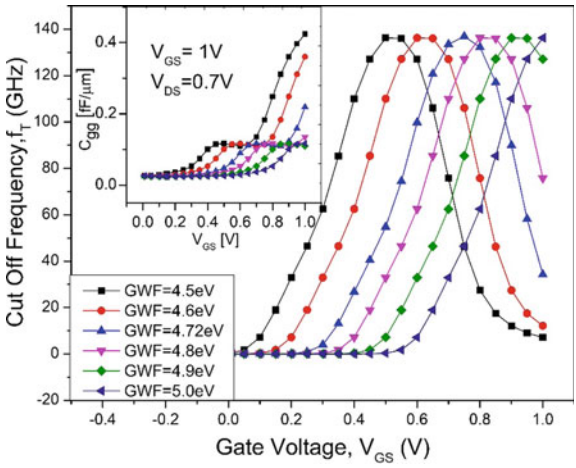

Fig. 7.22 f_t and (inset) C_{gg} as a function of V_{GS} for different φ_{ms}

Figure 7.23 presents the variation of the stability factor of the device against frequency for different gate work functions and critical frequency as function of gate work function (inset). The device exhibits better stability and smaller f_k for a low and moderate gate work function and both degrade with the further increase of gate work function. This is mainly due to the shift of $g_{m\,\max}$ as well $f_{t\max}$ and attaining maximum value at $V_{\mathrm{GS}} = 1$ V, when the gate work function is raised to 5 eV and impacting the stability factor and critical frequency.

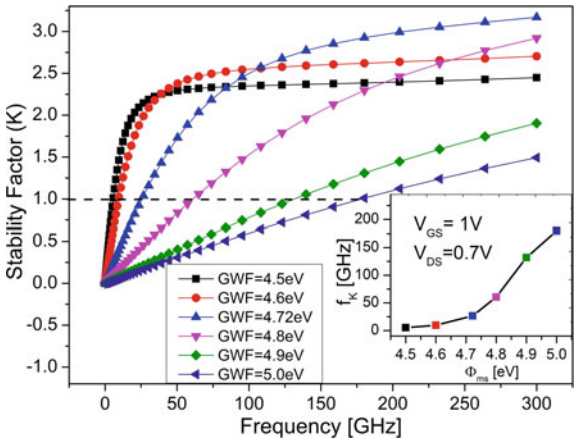

Fig. 7.23 Stability factor (K) as a function of frequency for different φ_{ms} and (inset) f_k as a function of φ_{ms}

7.6 Summary

In this chapter, the RF stability performance of SELBOX ITJLFET is reported. Impact of bias and geometrical parameters like channel length, SELBOX length, and underlap spacer length, fin height, and fin width variation on the RF stability of the device is discussed. From the simulation results, it can be concluded that the device stability is largely depending on the length of SELBOX. The stability factor of the device has been improved by 40%, and the critical frequency has reduced to 15 GHz from 26 GHz when the SELBOX length is changed from 10 to 40 nm. Moreover, it is noticed that the stability of the device is less sensitive to fin variations. To reduce the potentially unstable bandwidth and for better RF stability, the device should be operated with the following design guidelines. Bias voltages $V_{GS} \geq 1$ V and $V_{DS} \leq 0.7$ V and geometrical parameters like $L_G = 20$ nm, $L_{\text{SELBOX}} = 30$ nm, $L_{\text{US}} = 15$ nm, $H_{\text{fin}} = 30$ nm, and $W_{\text{fin}} = 10$ nm. These findings will be useful for RF designing and optimization of SELBOX ITJLFET when used as an RF amplifier.

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