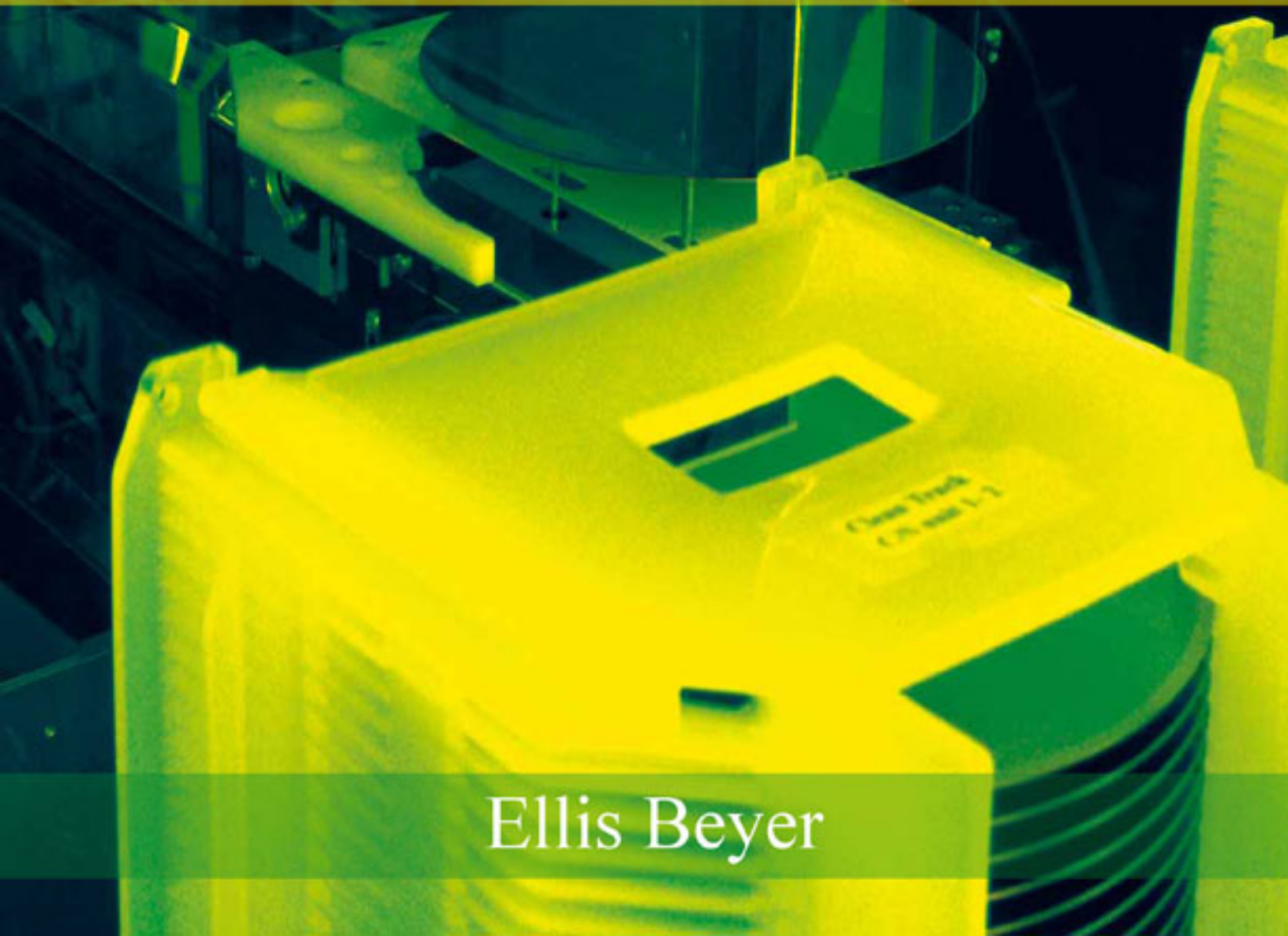
Semiconductor Technology



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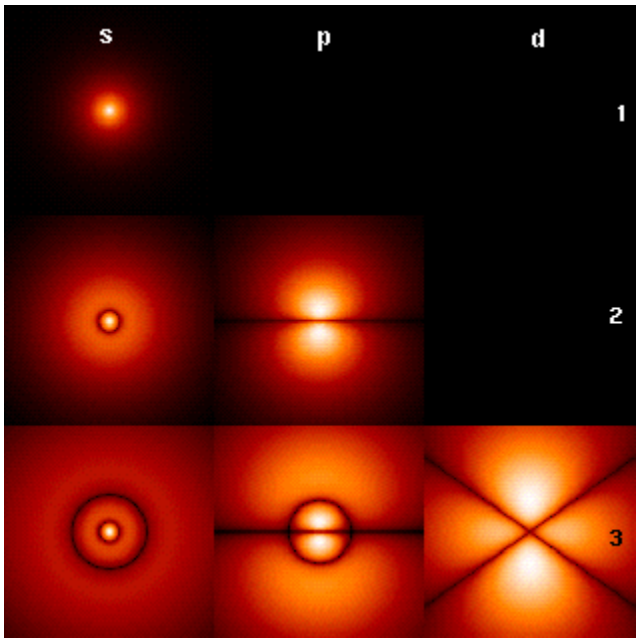
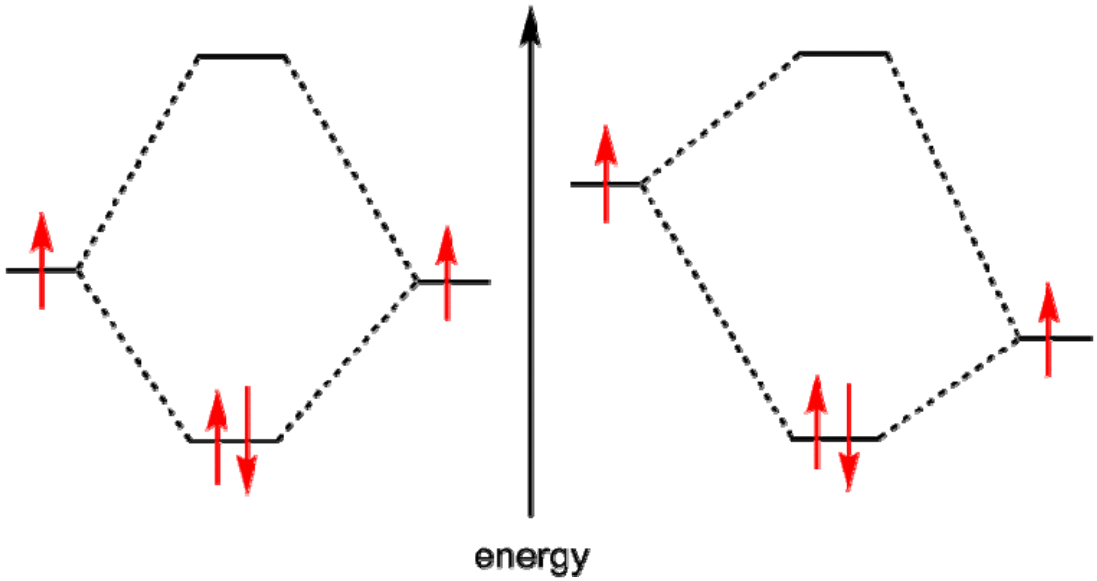
Introduction

A **semiconductor technology** is a technology with electrical conductivity due to electron flow (as opposed to ionic conductivity) intermediate in magnitude between that of a conductor and an insulator. This means a conductivity roughly in the range of 10^3 to 10^{-8} siemens per centimeter. Semiconductor materials are the foundation of modern electronics, including radio, computers, telephones, and many other devices. Such devices include transistors, solar cells, many kinds of diodes including the light-emitting diode, the silicon controlled rectifier, and digital and analog integrated circuits. Similarly, semiconductor solar photovoltaic panels directly convert light energy into electrical energy. In a metallic conductor, current is carried by the flow of electrons. In semiconductors, current is often schematized as being carried either by the flow of electrons or by the flow of positively charged "holes" in the electron structure of the material. Actually, however, in both cases only electron movements are involved.



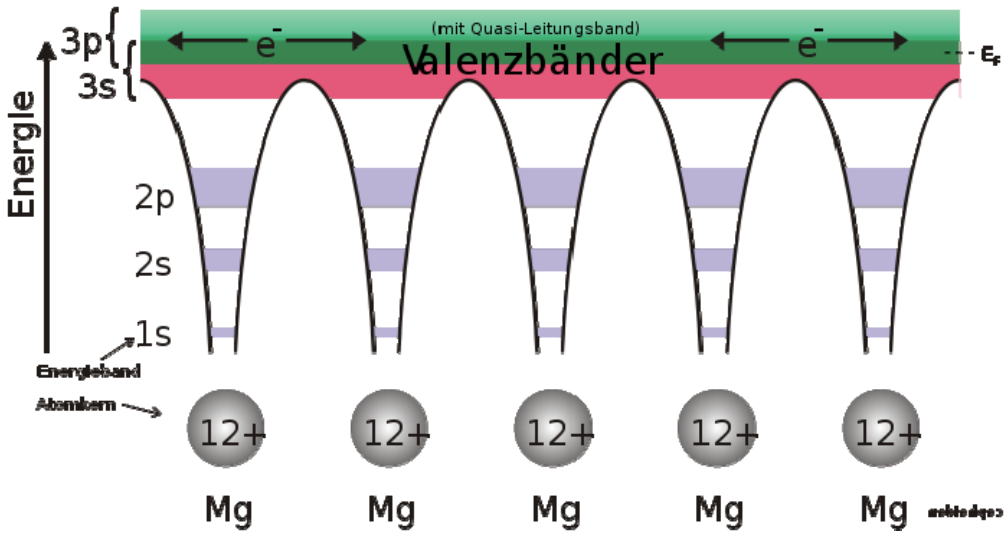
In a single H-atom an electron resides in well known orbitals. Note that the orbitals are called s,p,d in order of increasing circular current.

Common semiconducting materials are crystalline solids, but amorphous and liquid semiconductors are known. These include hydrogenated amorphous silicon and mixtures of arsenic, selenium and tellurium in a variety of proportions. Such compounds share with better known semiconductors intermediate conductivity and a rapid variation of conductivity with temperature, as well as occasional negative resistance. Such disordered materials lack the rigid crystalline structure of conventional semiconductors such as silicon and are generally used in thin film structures, which are less demanding for as concerns the electronic quality of the material and thus are relatively insensitive to impurities and radiation damage. Organic semiconductors, that is, organic materials with properties resembling conventional semiconductors, are also known.



Putting two atoms together leads to delocalized orbitals across two atoms, yielding a covalent bond. Due to the Pauli exclusion principle, every state can contain only one electron.

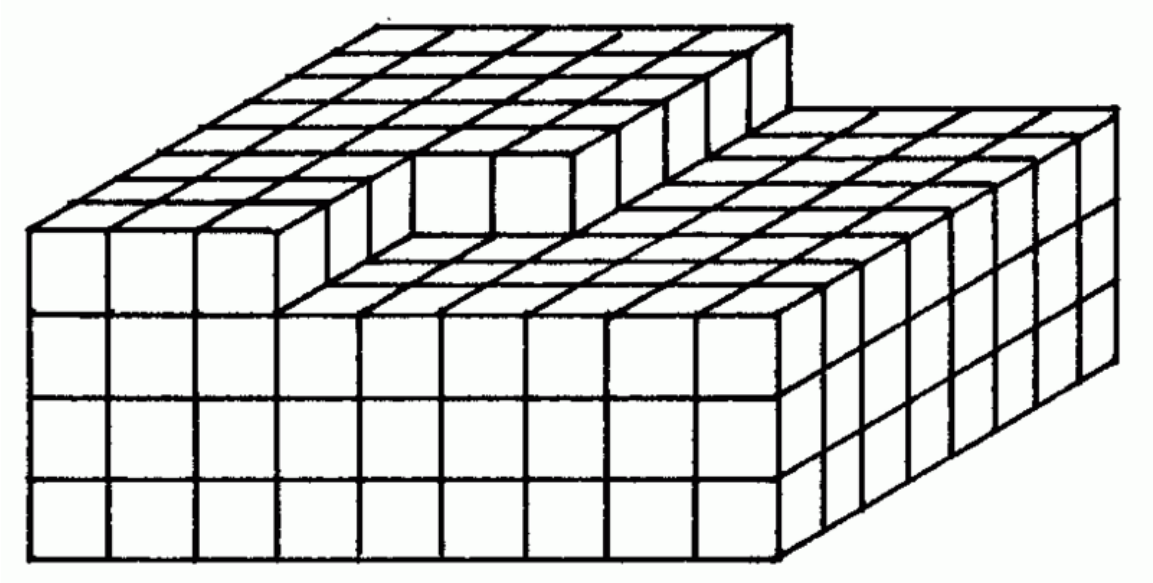
Silicon is used to create most semiconductors commercially. Dozens of other materials are used, including germanium, gallium arsenide, and silicon carbide. A pure semiconductor is often called an “intrinsic” semiconductor. The electronic properties and the conductivity of a semiconductor can be changed in a controlled manner by adding very small quantities of other elements, called “dopants”, to the intrinsic material. In crystalline silicon typically this is achieved by adding impurities of boron or phosphorus to the melt and then allowing the melt to solidify into the crystal. This process is called "doping".



This can be continued with more atoms. Note: This picture shows a metal, not an actual semiconductor.

Energy bands and electrical conduction

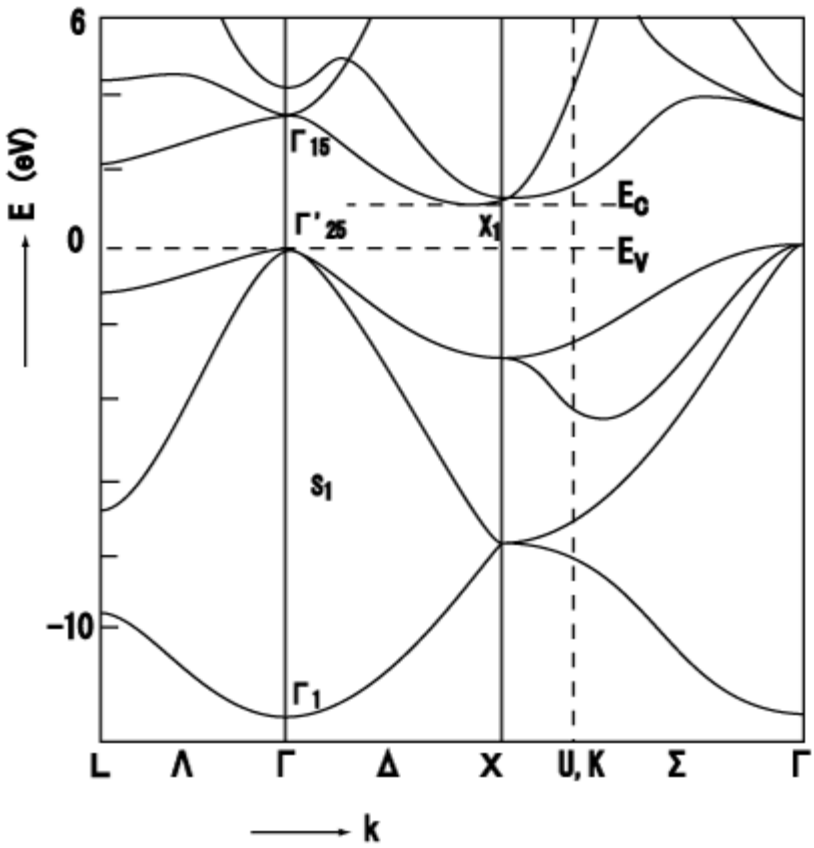
In classic crystalline semiconductors, the electrons can have energies only within certain bands (i.e. ranges of levels of energy). Energetically, these bands are located between the energy of the ground state, corresponding to electrons tightly bound to the atomic nuclei of the material, and the free electron energy. The latter is the energy required for an electron to escape entirely from the material. The energy bands each correspond to a large number of discrete quantum states of the electrons, and most of the states with low energy (closer to the nucleus) are full, up to a particular band called the *valence band*. Semiconductors and insulators are distinguished from metals because the valence band in them is nearly filled with electrons under usual operating conditions, while very few (semiconductor) or virtually none (insulator) of them are available in the *conduction band*, the band immediately above the valence band.



Continuing to add creates a crystal, which may then be cut into a tape and fused together at the ends to allow circular currents.

The ease with which electrons in a semiconductor can be excited from the valence band to the conduction band depends on the band gap between the bands. The size of this energy bandgap serves as an arbitrary dividing line (roughly 4 eV) between semiconductors and insulators.

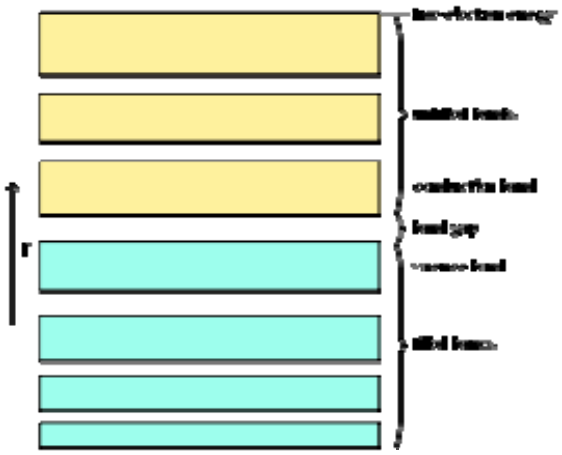
With covalent bonds, an electron moves by hopping to a neighboring bond. The Pauli exclusion principle requires the electron to be lifted into the higher anti-bonding state of that bond. For delocalized states, for example in one dimension – that is in a nanowire, for every energy there is a state with electrons flowing in one direction and another state with the electrons flowing in the other. For a net current to flow, more states for one direction than for the other direction must be occupied. For this to occur, energy is required, as in the semiconductor the next higher states lie above the band gap. Often this is stated as: full bands do not contribute to the electrical conductivity. However, as the temperature of a semiconductor rises above absolute zero, there is more energy in the semiconductor to spend on lattice vibration and — more importantly for us — on lifting some electrons into an energy states of the conduction band. The current-carrying electrons in the conduction band are known as "free electrons", although they are often simply called "electrons" if context allows this usage to be clear.



For this regular solid the band structure can be calculated or measured.

Electrons excited to the conduction band also leave behind electron holes, or unoccupied states in the valence band. Both the conduction band electrons and the valence band holes contribute to electrical conductivity. The holes themselves don't actually move, but a neighboring electron can move to fill the hole, leaving a hole at the place it has just come from, and in this way the holes appear to move, and the holes behave as if they were actual positively charged particles.

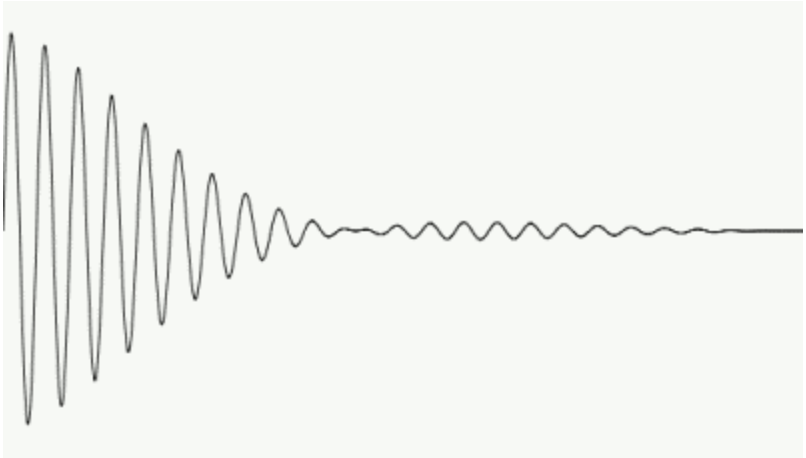
One covalent bond between neighboring atoms in the solid is ten times stronger than the binding of the single electron to the atom, so freeing the electron does not imply destruction of the crystal structure.



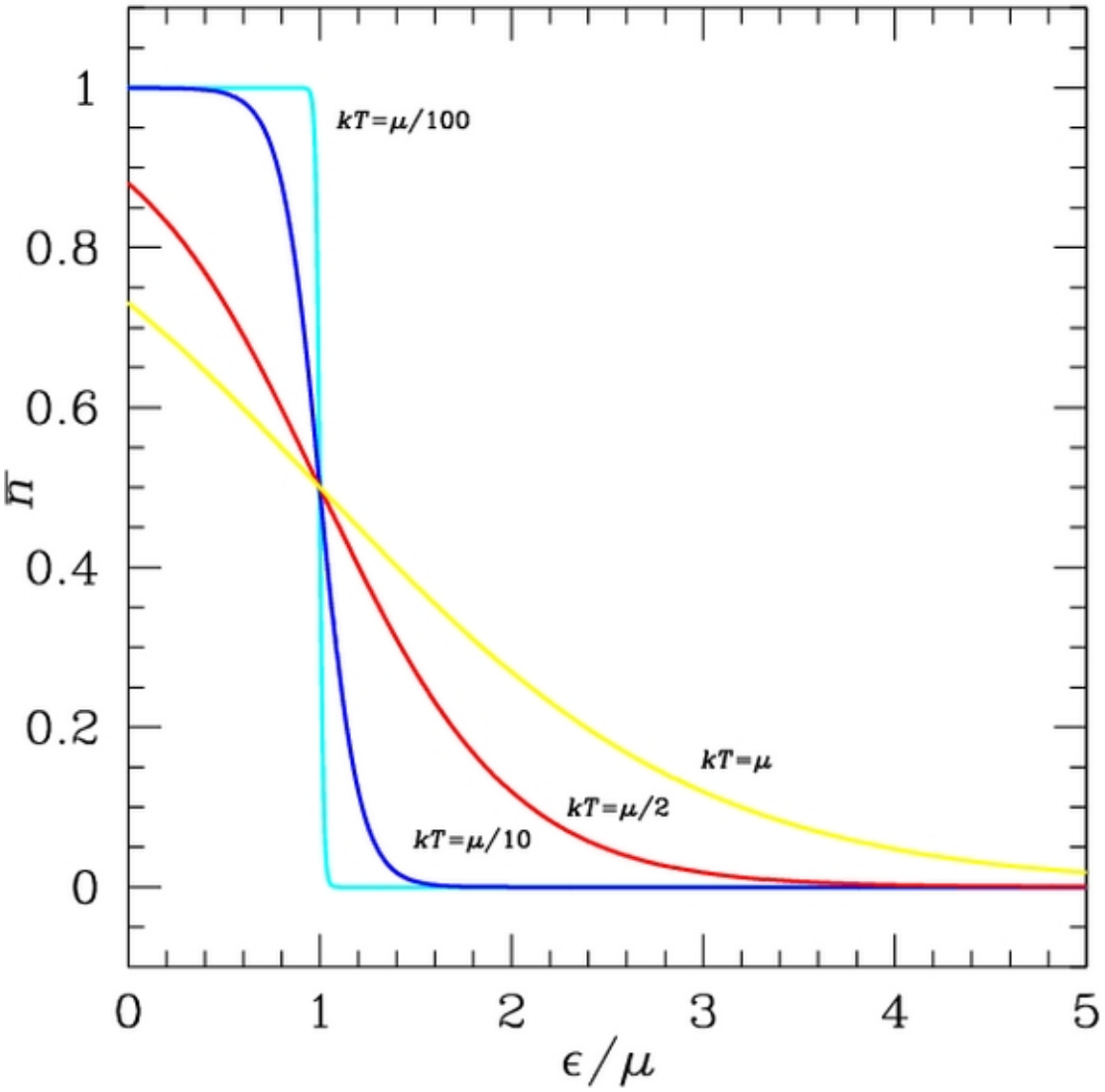
Integrating over the k axis gives the bands of a semiconductor showing a full valence band and an empty conduction band. Generally stopping at the vacuum level is undesirable, because some people want to calculate: photoemission, inverse photoemission

Holes: electron absence as a charge carrier

The concept of holes can also be applied to metals, where the Fermi level lies *within* the conduction band. With most metals the Hall effect indicates electrons are the charge carriers. However, some metals have a mostly filled conduction band. In these, the Hall effect reveals positive charge carriers, which are not the ion-cores, but holes. In the case of a metal, only a small amount of energy is needed for the electrons to find other unoccupied states to move into, and hence for current to flow. Sometimes even in this case it may be said that a hole was left behind, to explain why the electron does not fall back to lower energies: It cannot find a hole. In the end in both materials electron-phonon scattering and defects are the dominant causes for resistance.



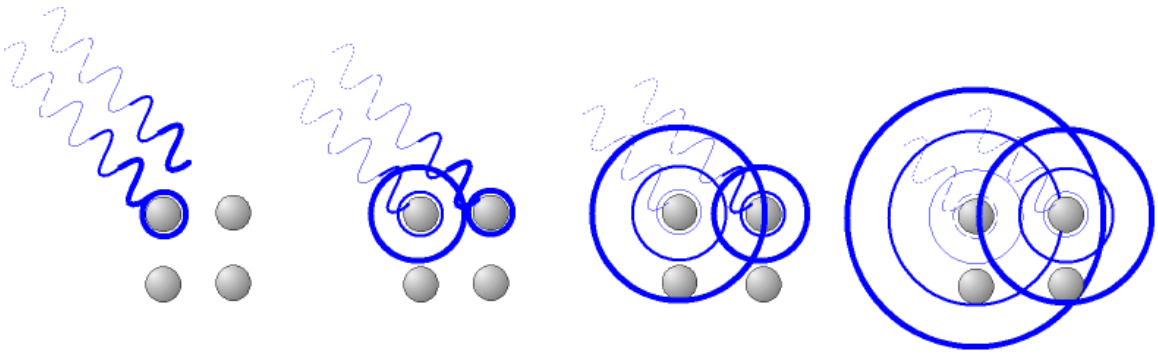
After the band structure is determined states can be combined to generate wave packets. As this is analogous to wave packages in free space, the results are similar.



Fermi-Dirac distribution. States with energy ε below the Fermi energy, here μ, have higher probability *n* to be occupied, and those above are less likely to be occupied. Smearing of the distribution increases with temperature.

The energy distribution of the electrons determines which of the states are filled and which are empty. This distribution is described by Fermi-Dirac statistics. The distribution is characterized by the temperature of the electrons, and the *Fermi energy* or *Fermi level*. Under absolute zero conditions the Fermi energy can be thought of as the energy up to

which available electron states are occupied. At higher temperatures, the Fermi energy is the energy at which the probability of a state being occupied has fallen to 0.5.



An alternative description, which does not really appreciate the strong Coulomb interaction, shoots free electrons into the crystal and looks at the scattering.

The dependence of the electron energy distribution on temperature also explains why the conductivity of a semiconductor has a strong temperature dependency, as a semiconductor operating at lower temperatures will have fewer available free electrons and holes able to do the work.

Energy–momentum dispersion

In the preceding description an important fact is ignored for the sake of simplicity: the *dispersion* of the energy. The reason that the energies of the states are broadened into a band is that the energy depends on the value of the wave vector, or *k-vector*, of the electron. The k-vector, in quantum mechanics, is the representation of the momentum of a particle.

The dispersion relationship determines the effective mass, m^*, of electrons or holes in the semiconductor, according to the formula:

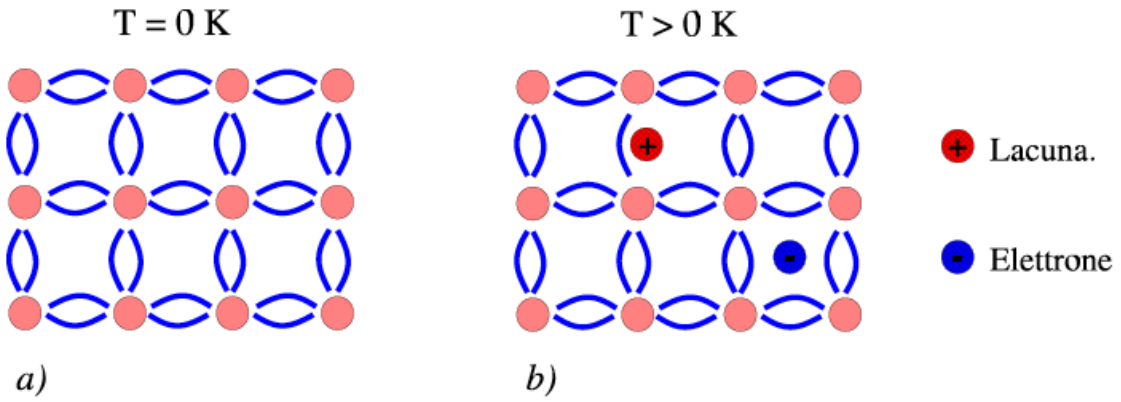
$$m^* = \hbar^2 \cdot \left[\frac{d^2 E(k)}{dk^2}\right]^{-1}.$$

The effective mass is important as it affects many of the electrical properties of the semiconductor, such as the electron or hole mobility, which in turn influences the *diffusivity* of the charge carriers and the electrical conductivity of the semiconductor.

Typically the effective mass of electrons and holes are different. This affects the relative performance of *p-channel* and *n-channel* IGFETs.

The top of the valence band and the bottom of the conduction band might not occur at that same value of *k*. Materials with this situation, such as silicon and germanium, are known as *indirect bandgap* materials. Materials in which the band extrema are aligned in

k, for example gallium arsenide, are called *direct bandgap* semiconductors. Direct gap semiconductors are particularly important in optoelectronics because they are much more efficient as light emitters than indirect gap materials.



A third alternative description uses strongly localized unpaired electrons in chemical bonds, which looks almost like a Mott insulator.

Carrier generation and recombination

When ionizing radiation strikes a semiconductor, it may excite an electron out of its energy level and consequently leave a hole. This process is known as *electron–hole pair generation*. Electron-hole pairs are constantly generated from thermal energy as well, in the absence of any external energy source.

Electron-hole pairs are also apt to recombine. Conservation of energy demands that these recombination events, in which an electron loses an amount of energy larger than the band gap, be accompanied by the emission of thermal energy (in the form of phonons) or radiation (in the form of photons).

In some states, the generation and recombination of electron–hole pairs are in equipoise. The number of electron-hole pairs in the steady state at a given temperature is determined by quantum statistical mechanics. The precise quantum mechanical mechanisms of generation and recombination are governed by conservation of energy and conservation of momentum.

As the probability that electrons and holes meet together is proportional to the product of their amounts, the product is in steady state nearly constant at a given temperature, providing that there is no significant electric field (which might "flush" carriers of both types, or move them from neighbour regions containing more of them to meet together) or externally driven pair generation. The product is a function of the temperature, as the probability of getting enough thermal energy to produce a pair increases with temperature, being approximately $\exp(-E_G/kT)$, where k is Boltzmann's constant, T is absolute temperature and E_G is band gap.

The probability of meeting is increased by carrier traps—impurities or dislocations which can trap an electron or hole and hold it until a pair is completed. Such carrier traps are sometimes purposely added to reduce the time needed to reach the steady state.

Semi-insulators

Some materials are classified as **semi-insulators**. These have electrical conductivity nearer to that of electrical insulators. Semi-insulators find niche applications in micro-electronics, such as substrates for HEMT. An example of a common semi-insulator is gallium arsenide.

Doping

The property of semiconductors that makes them most useful for constructing electronic devices is that their conductivity may easily be modified by introducing impurities into their crystal lattice. The process of adding controlled impurities to a semiconductor is known as *doping*. The amount of impurity, or dopant, added to an *intrinsic* (pure) semiconductor varies its level of conductivity. Doped semiconductors are often referred to as *extrinsic*. By adding impurity to pure semiconductors, the electrical conductivity may be varied not only by the number of impurity atoms but also, by the type of impurity atom and the changes may be thousand folds and million folds. For example, 1 cm^3 of a metal or semiconductor specimen has a number of atoms on the order of 10^{22}. Since every atom in metal donates at least one free electron for conduction in metal, 1 cm^3 of metal contains free electrons on the order of 10^{22}. At the temperature close to 20 °C , 1 cm^3 of pure germanium contains about 4.2×10^{22} atoms and 2.5×10^{13} free electrons and 2.5×10^{13} holes (empty spaces in crystal lattice having positive charge) The addition of 0.001% of arsenic (an impurity) donates an extra 10^{17} free electrons in the same volume and the electrical conductivity increases about 10,000 times."

Dopants

The materials chosen as suitable dopants depend on the atomic properties of both the dopant and the material to be doped. In general, dopants that produce the desired controlled changes are classified as either electron acceptors or donors. A donor atom that activates (that is, becomes incorporated into the crystal lattice) donates weakly bound valence electrons to the material, creating excess negative charge carriers. These weakly bound electrons can move about in the crystal lattice relatively freely and can facilitate conduction in the presence of an electric field. (The donor atoms introduce some states under, but very close to the conduction band edge. Electrons at these states can be easily excited to the conduction band, becoming free electrons, at room temperature.) Conversely, an activated acceptor produces a hole. Semiconductors doped with *donor* impurities are called *n-type*, while those doped with *acceptor* impurities are known as *p-type*. The n and p type designations indicate which charge carrier acts as the material's majority carrier. The opposite carrier is called the minority carrier, which exists due to thermal excitation at a much lower concentration compared to the majority carrier.

For example, the pure semiconductor silicon has four valence electrons. In silicon, the most common dopants are IUPAC group 13 (commonly known as *group III*) and group 15 (commonly known as *group V*) elements. Group 13 elements all contain three valence electrons, causing them to function as acceptors when used to dope silicon. Group 15 elements have five valence electrons, which allows them to act as a donor. Therefore, a silicon crystal doped with boron creates a p-type semiconductor whereas one doped with phosphorus results in an n-type material.

Carrier concentration

The concentration of dopant introduced to an intrinsic semiconductor determines its concentration and indirectly affects many of its electrical properties. The most important factor that doping directly affects is the material's carrier concentration. In an intrinsic semiconductor under thermal equilibrium, the concentration of electrons and holes is equivalent. That is,

$$n = p = n_i.$$

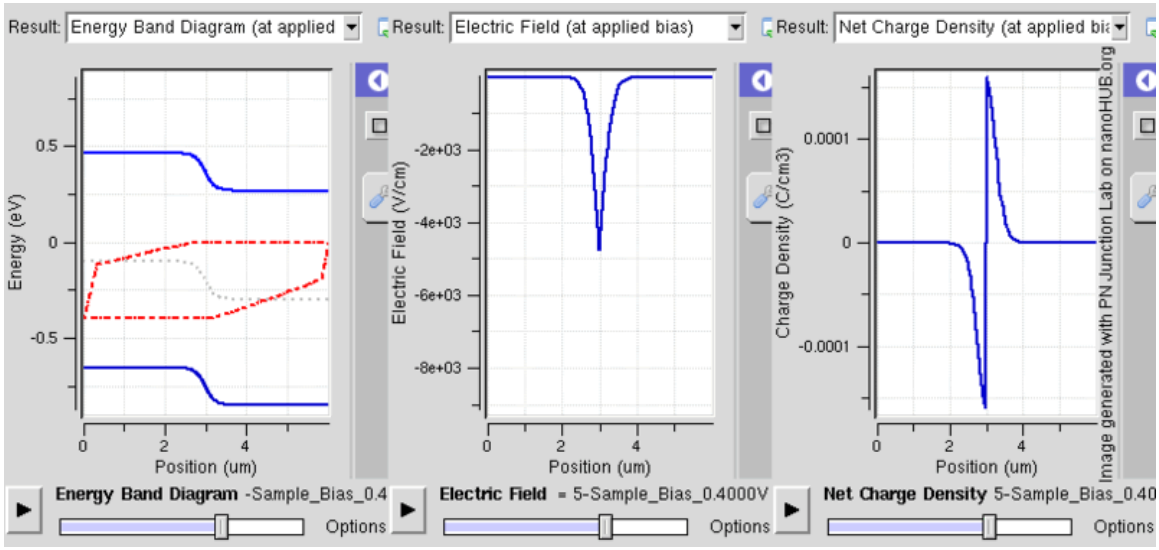
If we have a non-intrinsic semiconductor in thermal equilibrium the relation becomes:

$$n_0 \cdot p_0 = n_i^2$$

where n_0 is the concentration of conducting electrons, p_0 is the electron hole concentration, and n_i is the material's intrinsic carrier concentration. Intrinsic carrier concentration varies between materials and is dependent on temperature. Silicon's n_i, for example, is roughly 1.08×10^{10} cm^{-3} at 300 kelvins (room temperature).

In general, an increase in doping concentration affords an increase in conductivity due to the higher concentration of carriers available for conduction. Degenerately (very highly) doped semiconductors have conductivity levels comparable to metals and are often used in modern integrated circuits as a replacement for metal. Often superscript plus and minus symbols are used to denote relative doping concentration in semiconductors. For example, n^+ denotes an n-type semiconductor with a high, often degenerate, doping concentration. Similarly, p^- would indicate a very lightly doped p-type material. It is useful to note that even degenerate levels of doping imply low concentrations of impurities with respect to the base semiconductor. In crystalline intrinsic silicon, there are approximately 5×10^{22} atoms/cm^3. Doping concentration for silicon semiconductors may range anywhere from 10^{13} cm^{-3} to 10^{18} cm^{-3}. Doping concentration above about 10^{18} cm^{-3} is considered degenerate at room temperature. Degenerately doped silicon contains a proportion of impurity to silicon on the order of parts per thousand. This proportion may be reduced to parts per billion in very lightly doped silicon. Typical concentration values fall somewhere in this range and are tailored to produce the desired properties in the device that the semiconductor is intended for.

Effect on band structure



Band diagram of PN junction operation in forward bias mode showing reducing depletion width. Both p and n junctions are doped at a 1e15/cm3 doping level, leading to built-in potential of ~0.59V. Reducing depletion width can be inferred from the shrinking charge profile, as fewer dopants are exposed with increasing forward bias.

Doping a semiconductor crystal introduces allowed energy states within the band gap but very close to the energy band that corresponds to the dopant type. In other words, donor impurities create states near the conduction band while acceptors create states near the valence band. The gap between these energy states and the nearest energy band is usually referred to as dopant-site bonding energy or E_B and is relatively small. For example, the E_B for boron in silicon bulk is 0.045 eV, compared with silicon's band gap of about 1.12 eV. Because E_B is so small, it takes little energy to ionize the dopant atoms and create free carriers in the conduction or valence bands. Usually the thermal energy available at room temperature is sufficient to ionize most of the dopant.

Dopants also have the important effect of shifting the material's Fermi level towards the energy band that corresponds with the dopant with the greatest concentration. Since the Fermi level must remain constant in a system in thermodynamic equilibrium, stacking layers of materials with different properties leads to many useful electrical properties. For example, the p-n junction's properties are due to the energy band bending that happens as a result of lining up the Fermi levels in contacting regions of p-type and n-type material.

This effect is shown in a *band diagram*. The band diagram typically indicates the variation in the valence band and conduction band edges versus some spatial dimension, often denoted x. The Fermi energy is also usually indicated in the diagram. Sometimes the *intrinsic Fermi energy*, E_i, which is the Fermi level in the absence of doping, is shown. These diagrams are useful in explaining the operation of many kinds of semiconductor devices.

Preparation of semiconductor materials

Semiconductors with predictable, reliable electronic properties are necessary for mass production. The level of chemical purity needed is extremely high because the presence of impurities even in very small proportions can have large effects on the properties of the material. A high degree of crystalline perfection is also required, since faults in crystal structure (such as dislocations, twins, and stacking faults) interfere with the semiconducting properties of the material. Crystalline faults are a major cause of defective semiconductor devices. The larger the crystal, the more difficult it is to achieve the necessary perfection. Current mass production processes use crystal ingots between 100 mm and 300 mm (4–12 inches) in diameter which are grown as cylinders and sliced into wafers.

Because of the required level of chemical purity and the perfection of the crystal structure which are needed to make semiconductor devices, special methods have been developed to produce the initial semiconductor material. A technique for achieving high purity includes growing the crystal using the Czochralski process. An additional step that can be used to further increase purity is known as zone refining. In zone refining, part of a solid crystal is melted. The impurities tend to concentrate in the melted region, while the desired material recrystalizes leaving the solid material more pure and with fewer crystalline faults.

In manufacturing semiconductor devices involving heterojunctions between different semiconductor materials, the lattice constant, which is the length of the repeating element of the crystal structure, is important for determining the compatibility of materials.

Chapter- 2

Etching (Microfabrication)

Etching tanks used to perform Piranha, Hydrofluoric acid or RCA clean on 4-inch wafer batches at LAAS technological facility in Toulouse, France.

Etching is used in microfabrication to chemically remove layers from the surface of a wafer during manufacturing. Etching is a critically important process module, and every wafer undergoes many etching steps before it is complete.

For many etch steps, part of the wafer is protected from the etchant by a "masking" material which resists etching. In some cases, the masking material is a photoresist which

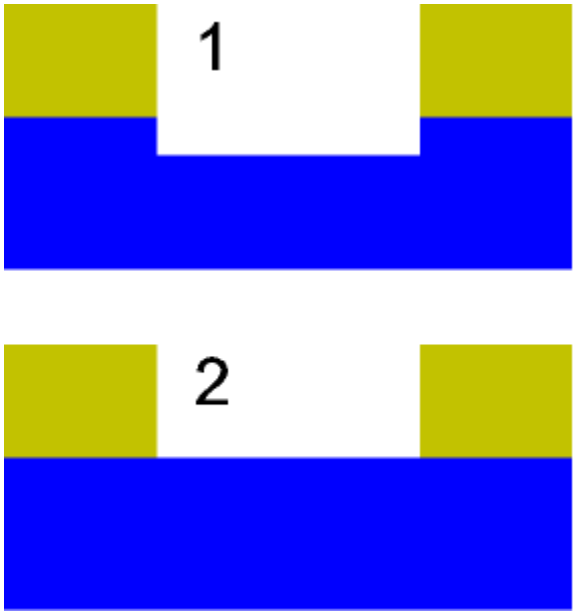
has been patterned using photolithography. Other situations require a more durable mask, such as silicon nitride.

Figures of merit

If the etch is intended to make a cavity in a material, the depth of the cavity may be controlled approximately using the etching time and the known etch rate. More often, though, etching must entirely remove the top layer of a multilayer structure, without damaging the underlying or masking layers. The etching system's ability to do this depends on the ratio of etch rates in the two materials (*selectivity*).

Some etches undercut the masking layer and form cavities with sloping sidewalls. The distance of undercutting is called *bias*. Etchants with large bias are called *isotropic*, because they erode the substrate equally in all directions. Modern processes greatly prefer anisotropic etches, because they produce sharp, well-controlled features.

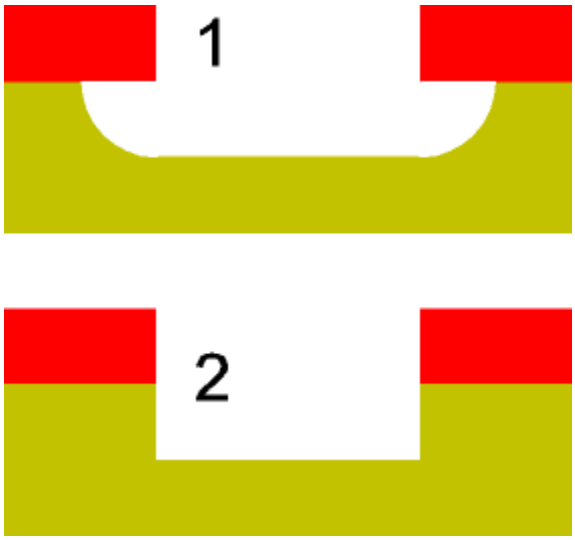
Selectivity



Yellow: layer to be removed; blue: layer to remain

1. A poorly selective etch removes the top layer, but also attacks the underlying material.
2. A highly selective etch leaves the underlying material unharmed.

Isotropy



Red: masking layer; yellow: layer to be removed

1. A perfectly isotropic etch produces round sidewalls.
2. A perfectly anisotropic etch produces vertical sidewalls.

Etching media and technology

The two fundamental types of etchants are liquid-phase ("wet") and plasma-phase ("dry"). Each of these exists in several varieties.

Wet etching

The first etching processes used liquid-phase ("wet") etchants. The wafer can be immersed in a bath of etchant, which must be agitated to achieve good process control. For instance, buffered hydrofluoric acid (BHF) is used commonly to etch silicon dioxide over a silicon substrate.

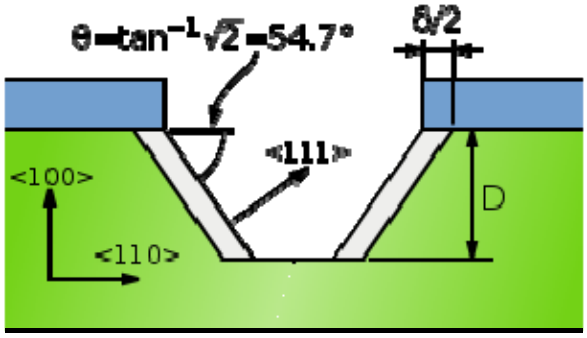
Different specialised etchants can be used to characterise the surface etched.

Wet etchants are usually isotropic, which leads to large bias when etching thick films. They also require the disposal of large amounts of toxic waste. For these reasons, they are seldom used in state-of-the-art processes. However, the photographic developer used for photoresist resembles wet etching.

As an alternative to immersion, single wafer machines use the Bernoulli principle to employ a gas (usually, pure nitrogen) to cushion and protect one side of the wafer while etchant is applied to the other side. It can be done to either the front side or back side. The etch chemistry is dispensed on the top side when in the machine and the bottom side is not affected. This etch method is particularly effective just before "backend" processing (BEOL), where wafers are normally very much thinner after wafer backgrinding, and very sensitive to thermal or mechanical stress. Etching a thin layer of

even a few micrometres will remove microcracks produced during backgrinding resulting in a the wafer having dramatically increased strength and flexibility without breaking.

Anisotropic wet etching



An anisotropic wet etch on a silicon wafer creates a cavity with a trapezoidal cross-section. The bottom of the cavity is a <100> plane, and the sides are <111> planes. The blue material is an etch mask, and the green material is silicon.

Some wet etchants etch crystalline materials at very different rates depending upon which crystal face is exposed. In single-crystal materials (e.g. silicon wafers), this effect can allow very high anisotropy, as shown in the figure.

Several anisotropic wet etchants are available for silicon. For instance, potassium hydroxide (KOH) can achieve selectivity of 400 between <100> and <111> planes. Another option is EDP (an aqueous solution of ethylene diamine and pyrocatechol), which also displays high selectivity for p-type doping. Neither of these etchants may be used on wafers that contain CMOS integrated circuits. Both of them etch aluminum, commonly used as a metallization (wiring) material. KOH introduces mobile potassium ions into silicon dioxide, and EDP is highly corrosive and carcinogenic. Tetramethylammonium hydroxide (TMAH) presents a safer alternative, although it has even worse selectivity between <100> and <111> planes in silicon than does EDP.

Etching a rectangular hole in a (100)-Si wafer will result in a pyramid shaped etch pit. The wall will be flat and angled (as opposed to curved in isotropic etching), and have an angle to the surface of the wafer of:

$$\tan^{-1}\sqrt{2} = 54.7^\circ$$

If the etching is stopped before the pyramid is formed, a frustum will be formed. The undercut, δ, under the resist mask is given by:

$$\delta = \frac{\sqrt{6}D}{S} = \frac{\sqrt{6}R_{100}T}{R_{100}/R_{111}} = \sqrt{6}TR_{111},$$

where R_{xxx} is the etch rate in the <xxx> direction, T is the etch time, D is the etch depth and S is the anisotropy of the material and etchant.

Different etchants have different anisotropies. Below is a table of common anisotropic etchants for silicon:

Etchant	Operating temp (°C)	R_{100} (μm/min)	$S=R_{100}/R_{111}$	Mask materials
Ethylenediamine pyrocatechol (EDP)	110	0.47	17	SiO_2, Si_3N_4, Au, Cr, Ag, Cu
Potassium hydroxide/Isopropyl alcohol (KOH/IPA)	50	1.0	400	Si_3N_4, SiO_2 (etches at 140nm/min)
Tetramethylammonium hydroxide (TMAH)	80	0.6	37	Si_3N_4, SiO_2

Plasma etching

Modern VLSI processes avoid wet etching, and use *plasma etching* instead. Plasma etchers can operate in several modes by adjusting the parameters of the plasma. Ordinary plasma etching operates between 0.1 and 5 Torr. (This unit of pressure, commonly used in vacuum engineering, equals approximately 133.3 pascals.) The plasma produces energetic free radicals, neutrally charged, that react at the surface of the wafer. Since neutral particles attack the wafer from all angles, this process is isotropic.

The source gas for the plasma usually contains small molecules rich in chlorine or fluorine. For instance, carbon tetrachloride (CCl_4) etches silicon and aluminium, and trifluoromethane etches silicon dioxide and silicon nitride. A plasma containing oxygen is used to oxidize ("ash") photoresist and facilitate its removal.

Ion milling, or *sputter etching*, uses lower pressures, often as low as 10^{-4} Torr (10 mPa). It bombards the wafer with energetic ions of noble gases, often Ar^+, which knock atoms from the substrate by transferring momentum. Because the etching is performed by ions, which approach the wafer approximately from one direction, this process is highly anisotropic. On the other hand, it tends to display poor selectivity. *Reactive-ion etching*

(RIE) operates under conditions intermediate between sputter and plasma etching (between 10^{-3} and 10^{-1} Torr). *Deep reactive-ion etching* (DRIE) modifies the RIE technique to produce deep, narrow features.

Common etch processes used in microfabrication

Etchants for common microfabrication materials

Material to be etched	Wet etchants	Plasma etchants
Aluminium (Al)	80% phosphoric acid (H_3PO_4) + 5% acetic acid + 5% nitric acid (HNO_3) + 10% water (H_2O) at 35–45 °C	Cl_2, CCl_4, $SiCl_4$, BCl_3
Indium tin oxide [ITO] (In_2O_3:SnO_2)	Hydrochloric acid (HCl) + nitric acid (HNO_3) + water (H_2O) (1:0.1:1) at 40 °C	
Chromium (Cr)	• "Chrome etch": ceric ammonium nitrate ($(NH_4)_2Ce(NO_3)_6$) + nitric acid (HNO_3) • Hydrochloric acid (HCl)	
Gold (Au)	Aqua regia	
Molybdenum (Mo)		CF_4
Organic residues and photoresist	Piranha etch: sulfuric acid (H_2SO_4) + hydrogen peroxide (H_2O_2)	O_2 (ashing)
Platinum (Pt)	Aqua regia	
Silicon (Si)	Nitric acid (HNO_3) + hydrofluoric acid (HF)	• CF_4, SF_6, NF_3 • Cl_2, CCl_2F_2
Silicon dioxide (SiO_2)	• Hydrofluoric acid (HF) • Buffered oxide etch [BOE]: ammonium fluoride (NH_4F) and hydrofluoric acid (HF)	CF_4, SF_6, NF_3
Silicon nitride (Si_3N_4)	• 85% Phosphoric acid (H_3PO_4) at 180 °C (Requires SiO_2 etch mask)	CF_4, SF_6, NF_3

Tantalum (Ta)		CF_4
Titanium (Ti)	Hydrofluoric acid (HF)	BCl_3
Titanium nitride (TiN)	• Nitric acid (HNO_3) + hydrofluoric acid (HF) • SC1	
Tungsten (W)	• Nitric acid (HNO_3) + hydrofluoric acid (HF) • Hydrogen Peroxide (H_2O_2)	• CF_4 • SF_6

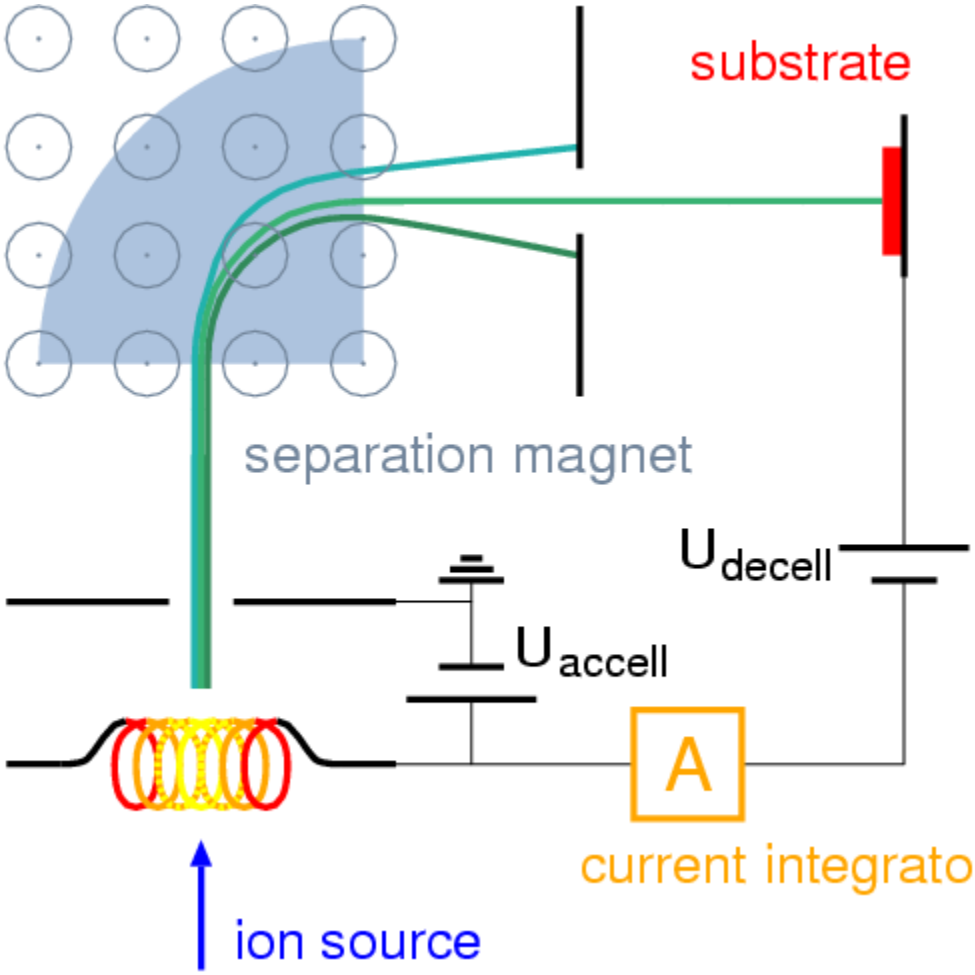
Chapter- 3

Ion Implantation

An ion implantation system at LAAS technological facility in Toulouse, France.

Ion implantation is a materials engineering process by which ions of a material can be implanted into another solid, thereby changing the physical properties of the solid. Ion implantation is used in semiconductor device fabrication and in metal finishing, as well as various applications in materials science research. The ions introduce both a chemical change in the target, in that they can be a different element than the target or induce a nuclear transmutation, and a structural change, in that the crystal structure of the target can be damaged or even destroyed by the energetic collision cascades.

General principle



Ion implantation setup with mass separator

Ion implantation equipment typically consists of an ion source, where ions of the desired element are produced, an accelerator, where the ions are electrostatically accelerated to a high energy, and a target chamber, where the ions impinge on a target, which is the material to be implanted. Thus ion implantation is a special case of particle radiation. Each ion is typically a single atom or molecule, and thus the actual amount of material implanted in the target is the integral over time of the ion current. This amount is called the dose. The currents supplied by implanters are typically small (microamperes), and thus the dose which can be implanted in a reasonable amount of time is small. Therefore,

ion implantation finds application in cases where the amount of chemical change required is small.

Typical ion energies are in the range of 10 to 500 keV (1,600 to 80,000 aJ). Energies in the range 1 to 10 keV (160 to 1,600 aJ) can be used, but result in a penetration of only a few nanometers or less. Energies lower than this result in very little damage to the target, and fall under the designation ion beam deposition. Higher energies can also be used: accelerators capable of 5 MeV (800,000 aJ) are common. However, there is often great structural damage to the target, and because the depth distribution is broad, the net composition change at any point in the target will be small.

The energy of the ions, as well as the ion species and the composition of the target determine the depth of penetration of the ions in the solid: A monoenergetic ion beam will generally have a broad depth distribution. The average penetration depth is called the range of the ions. Under typical circumstances ion ranges will be between 10 nanometers and 1 micrometer. Thus, ion implantation is especially useful in cases where the chemical or structural change is desired to be near the surface of the target. Ions gradually lose their energy as they travel through the solid, both from occasional collisions with target atoms (which cause abrupt energy transfers) and from a mild drag from overlap of electron orbitals, which is a continuous process. The loss of ion energy in the target is called stopping and can be simulated with the binary collision approximation method.

Application in semiconductor device fabrication

Doping

The introduction of dopants in a semiconductor is the most common application of ion implantation. Dopant ions such as boron, phosphorus or arsenic are generally created from a gas source, so that the purity of the source can be very high. These gases tend to be very hazardous. When implanted in a semiconductor, each dopant atom can create a charge carrier in the semiconductor after annealing. A hole can be created for a p-type dopant, and an electron for an n-type dopant. This modifies the conductivity of the semiconductor in its vicinity. The technique is used, for example, for adjusting the threshold of a MOSFET.

Ion implantation was developed as a method of producing the p-n junction of photovoltaic devices in the late 1970s and early 1980s, along with the use of pulsed-electron beam for rapid annealing, although it has not to date been used for commercial production.

Silicon on insulator

One prominent method for preparing silicon on insulator (SOI) substrates from conventional silicon substrates is the *SIMOX* (**S**eparation by **IM**plantation of **OX**ygen) process, wherein a buried high dose oxygen implant is converted to silicon oxide by a high temperature annealing process.

Mesotaxy

Mesotaxy is the term for the growth of a crystallographically matching phase underneath the surface of the host crystal (compare to epitaxy, which is the growth of the matching phase on the surface of a substrate). In this process, ions are implanted at a high enough energy and dose into a material to create a layer of a second phase, and the temperature is controlled so that the crystal structure of the target is not destroyed. The crystal orientation of the layer can be engineered to match that of the target, even though the exact crystal structure and lattice constant may be very different. For example, after the implantation of nickel ions into a silicon wafer, a layer of nickel silicide can be grown in which the crystal orientation of the silicide matches that of the silicon.

Application in metal finishing

Tool steel toughening

Nitrogen or other ions can be implanted into a tool steel target (drill bits, for example). The structural change caused by the implantation produces a surface compression in the steel, which prevents crack propagation and thus makes the material more resistant to fracture. The chemical change can also make the tool more resistant to corrosion.

Surface finishing

In some applications, for example prosthetic devices such as artificial joints, it is desired to have surfaces very resistant to both chemical corrosion and wear due to friction. Ion implantation is used in such cases to engineer the surfaces of such devices for more reliable performance. As in the case of tool steels, the surface modification caused by ion implantation includes both a surface compression which prevents crack propagation and an alloying of the surface to make it more chemically resistant to corrosion.

Other applications

Ion beam mixing

Ion implantation can be used to achieve ion beam mixing, i.e. mixing up atoms of different elements at an interface. This may be useful for achieving graded interfaces or strengthening adhesion between layers of immiscible materials.

Problems with ion implantation

Crystallographic damage

Each individual ion produces many point defects in the target crystal on impact such as vacancies and interstitials. Vacancies are crystal lattice points unoccupied by an atom: in this case the ion collides with a target atom, resulting in transfer of a significant amount of energy to the target atom such that it leaves its crystal site. This target atom then itself

becomes a projectile in the solid, and can cause successive collision events. Interstitials result when such atoms (or the original ion itself) come to rest in the solid, but find no vacant space in the lattice to reside. These point defects can migrate and cluster with each other, resulting in dislocation loops and other defects.

Damage recovery

Because ion implantation causes damage to the crystal structure of the target which is often unwanted, ion implantation processing is often followed by a thermal annealing. This can be referred to as damage recovery.

Amorphization

The amount of crystallographic damage can be enough to completely amorphize the surface of the target: i.e. it can become an amorphous solid (such a solid produced from a melt is called a glass). In some cases, complete amorphization of a target is preferable to a highly defective crystal: An amorphized film can be regrown at a lower temperature than required to anneal a highly damaged crystal.

Sputtering

Some of the collision events result in atoms being ejected (sputtered) from the surface, and thus ion implantation will slowly etch away a surface. The effect is only appreciable for very large doses.

Ion channelling

A diamond cubic crystal viewed from the <110> direction, showing hexagonal ion channels.

If there is a crystallographic structure to the target, and especially in semiconductor substrates where the crystal structure is more open, particular crystallographic directions offer much lower stopping than other directions. The result is that the range of an ion can be much longer if the ion travels exactly along a particular direction, for example the <110> direction in silicon and other diamond cubic materials. This effect is called *ion channelling*, and, like all the channelling effects, is highly nonlinear, with small variations from perfect orientation resulting in extreme differences in implantation depth. For this reason, most implantation is carried out a few degrees off-axis, where tiny alignment errors will have more predictable effects.

Ion channelling can be used directly in Rutherford backscattering and related techniques as an analytical method to determine the amount and depth profile of damage in crystalline thin film materials.

Hazardous Materials Note

In the ion implantation semiconductor fabrication process of wafers, it is important for the workers to minimize their exposure to the toxic materials used in the ion implanter process. Such hazardous elements, solid source and gasses are used, such as Arsine and Phosphine. For this reason, the semiconductor fabrication facilities are highly automated, and may feature negative pressure gas bottles safe delivery system (SDS). Other elements may include Antimony, Arsenic, Phosphorus, and Boron. Residue of these elements show up when the machine is opened to atmosphere, and can also be accumulated and found concentrated in the vacuum pumps hardware. It is important not to expose yourself to these carcinogenic, corrosive, flammable, and toxic elements. Many overlapping safety protocols must be used when handling these deadly compounds. Use safety, and read MSDS's.

High Voltage Safety

High voltage power supplies in ion implantation equipment can pose a risk of electrocution. In addition, high-energy atomic collisions can, in some cases, generate radionuclides. Operators and Maintenance personnel should learn and follow the safety advice of the manufacturer and/or the institution responsible for the equipment. Prior to entry to high voltage area, terminal components must be grounded using a grounding stick. Next, power supplies should be locked in the off state and tagged to prevent unauthorized energizing.

Chapter- 4

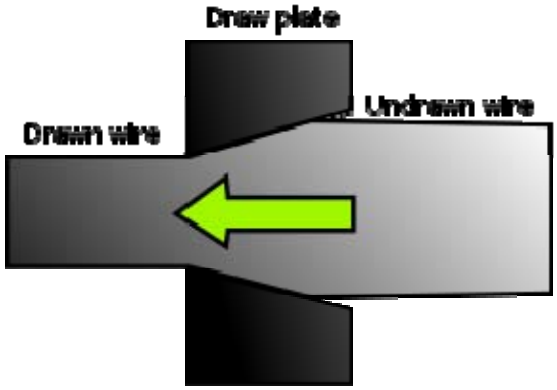
Wire Drawing

Drawing silver wire by hand pulling.

Drawing thicker silver wire by cranked pulling.

Wire drawing is a metalworking process used to reduce the cross-section of a wire by pulling the wire through a single, or series of, drawing die(s). There are many applications for wire drawing, including electrical wiring, cables, tension-loaded structural components, springs, paper clips, spokes for wheels, and stringed musical instruments. Although similar in process, drawing is different from extrusion, because in drawing the wire is pulled, rather than pushed, through the die. Drawing is usually performed at room temperature, thus classified a cold working process, but it may be performed at elevated temperatures for large wires to reduce forces. More recently drawing has been used with molten glass to produce high quality optical fibers.

Process



Wire drawing concept

The wire drawing process is quite simple in concept. The wire is prepared by shrinking the beginning of it, by hammering, filing, rolling or swaging, so that it will fit through the die; the wire is then pulled through the die. As the wire is pulled through the die, its volume remains the same, so as the diameter decreases, the length increases. Usually the wire will require more than one draw, through successively smaller dies, to reach the desired size. The American wire gauge scale is based on this. This can be done on a small scale with a draw plate, or on a large commercial scale using automated machinery. The process of wire drawing improves material properties due to cold working.

The areal reduction of small wires are 15–25% and larger wires are 20–45%. Very fine wires are usually drawn in bundles. In a bundle, the wires are separated by a metal with similar properties, but with lower chemical resistance so that it can be removed after drawing. If the reduction in diameter is greater than 50%, the process may require annealing between the process of drawing the wire through the dies. Commercial wire drawing usually starts with a coil of hot rolled 9 mm (0.35 in) diameter wire. The surface is first treated to remove scales. It is then fed into either a single block or continuous wire drawing machine.

Single block wire drawing machines include means for holding the dies accurately in position and for drawing the wire steadily through the holes. The usual design consists of a cast-iron bench or table having a bracket standing up to hold the die, and a vertical drum which rotates and by coiling the wire around its surface pulls it through the die, the coil of wire being stored upon another drum or "swift" which lies behind the die and reels off the wire as fast as required. The wire drum or "block" is provided with means for rapidly coupling or uncoupling it to its vertical shaft, so that the motion of the wire may be stopped or started instantly. The block is also tapered, so that the coil of wire may be easily slipped off upwards when finished. Before the wire can be attached to the block, a sufficient length of it must be pulled through the die; this is effected by a pair of gripping pincers on the end of a chain which is wound around a revolving drum, so drawing the wire until enough can be coiled two or three times on the block, where the end is secured by a small screw clamp or vice. When the wire is on the block, it is set in motion and the wire is drawn steadily through the die; it is very important that the block rotates evenly

and that it runs true and pulls the wire at a constant velocity, otherwise "snatching" occurs which will weaken or even break the wire. The speeds at which wire is drawn vary greatly, according to the material and the amount of reduction.

Continuous wire drawing machines differ from the single block machines in having a series of dies through which the wire passes in a continuous manner. The difficulty of feeding between each die is solved by introducing a block between each die. The speeds of the blocks are increased successively, so that the elongation is taken up and any slip compensated for. One of these machines may contain 3 to 12 dies. The operation of threading the wire through all the dies and around the blocks is termed "stringing-up". The arrangements for lubrication include a pump which floods the dies, and in many cases also the bottom portions of the blocks run in lubricant.

Often intermediate anneals are required to counter the effects of cold working, and to allow more further drawing. A final anneal may also be used on the finished product to maximize ductility and electrical conductivity.

An example of product produced in a continuous wire drawing machine is telephone wire. It is drawn 20 to 30 times from hot rolled rod stock.

While round cross-sections dominate most drawing processes, non-circular cross-sections are drawn. They are usually drawn when the cross-section is small and quantities are too low to justify rolling. In these processes, a block or Turk's-head machine are used.

Lubrication

Lubrication in the drawing process is essential for maintaining good surface finish and long die life. The following are different methods of lubrication:

- Wet drawing: the dies and wire or rod are completely immersed in lubricant
- Dry drawing: the wire or rod passes through a container of lubricant which coats the surface of the wire or rod
- Metal coating: the wire or rod is coated with a soft metal which acts as a solid lubricant
- Ultrasonic vibration: the dies and mandrels are vibrated, which helps to reduce forces and allow larger reductions per pass

Various lubricants, such as oil, are employed. Another lubrication method is to immerse the wire in a copper (II) sulfate solution, such that a film of copper is deposited which forms a kind of lubricant. In some classes of wire the copper is left after the final drawing to serve as a preventive of rust or to allow easy soldering.

Mechanical Properties

The strength-enhancing effect of wire drawing can be substantial. The highest tensile strengths available on any steel have been recorded on small-diameter cold-drawn austenitic stainless wire. Tensile strength can be as high as 400 ksi (3760 MPa).

Drawing dies

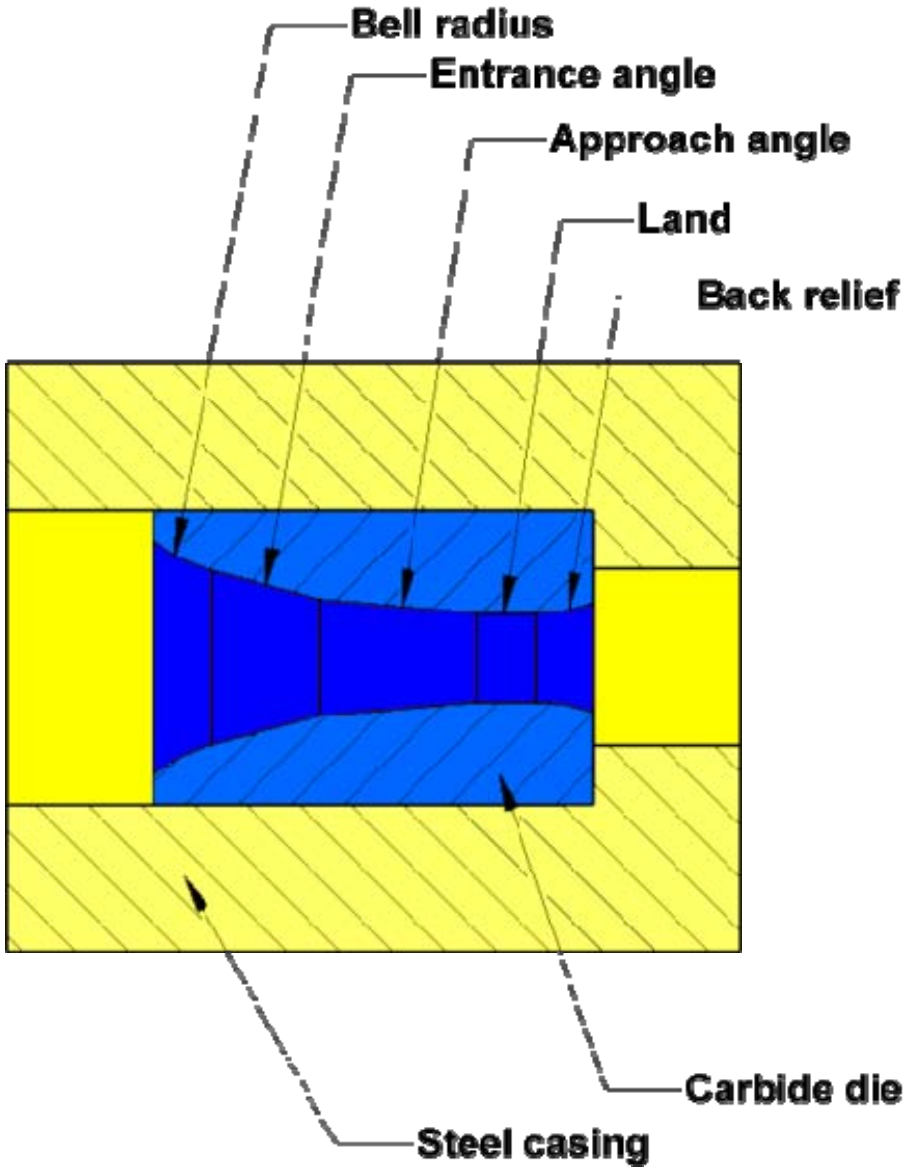


Diagram of a carbide wire drawing die

Drawing dies are typically made of tool steel, tungsten carbide, or diamond, with tungsten carbide and manufactured diamond being the most common. Synthetic diamond is usually used in the early stages of the drawing process, whereas natural diamond dies

are used in the final stages. For drawing very fine wire a single crystal diamond die is used. For hot drawing, cast-steel dies are used. For steel wire drawing, a tungsten carbide die is used. The dies are placed in a steel casing, which backs the die and allow for easy die changes. Die angles usually range from 6–15°, and each die has at least 2 different angles: the entering angle and approach angle. Wire dies usually are used with power as to pull the wire through them. There are coils of wire on either end of the die which pull and roll up the wire with a reduced diameter.

Chapter- 5

Thermal Oxidation & Thermal Management of High-Power LEDs

Thermal oxidation

Furnaces used for diffusion and thermal oxidation at LAAS technological facility in Toulouse, France.

In microfabrication, **thermal oxidation** is a way to produce a thin layer of oxide (usually silicon dioxide) on the surface of a wafer (semiconductor). The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it. The rate of oxide growth is often predicted by the Deal-Grove model.

The chemical reaction

Thermal oxidation of silicon is usually performed at a temperature between 800 and 1200°C, resulting in so called **High Temperature Oxide** layer (HTO). It may use either water vapor (steam) or molecular oxygen as the oxidant; it is consequently called either *wet* or *dry* oxidation. The reaction is one of the following:

$$\mathrm{Si} + 2\mathrm{H_2O} \rightarrow \mathrm{SiO_2} + 2\mathrm{H_2}$$
$$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2}$$

The oxidizing ambient may also contain several percent of hydrochloric acid (HCl). The chlorine removes metal ions that may occur in the oxide.

Thermal oxide incorporates silicon consumed from the substrate and oxygen supplied from the ambient. Thus, it grows both down into the wafer and up out of it. For every unit thickness of silicon consumed, 2.27 unit thicknesses of oxide will appear . Conversely, if a bare silicon surface is oxidized, 46% of the oxide thickness will lie below the original surface, and 54% above it.

Deal-Grove model

According to the commonly-used Deal-Grove model, the time *t* required to grow an oxide of thickness X_o, at a constant temperature, on a bare silicon surface, is:

$$t = \frac{X_o^2}{B} + \frac{X_o}{B/A}$$

where the constants A and B encapsulate the properties of the reaction and the oxide layer, respectively.

If a wafer that already contains oxide is placed in an oxidizing ambient, this equation must be modified by adding a corrective term τ, the time that would have been required to grow the pre-existing oxide under current conditions. This term may be found using the equation for *t* above.

Solving the quadratic equation for X_o yields:

$$X_o(t) = A/2 \cdot \left[\sqrt{1 + \frac{4B}{A^2}(t+\tau)} - 1\right]$$

Oxidation technology

Most thermal oxidation is performed in furnaces, at temperatures between 800 and 1200°C. A single furnace accepts many wafers at the same time, in a specially designed quartz rack (called a "boat"). Historically, the boat entered the oxidation chamber from the side (this design is called "horizontal"), and held the wafers vertically, beside each other. However, many modern designs hold the wafers horizontally, above and below each other, and load them into the oxidation chamber from below.

Vertical furnaces stand higher than horizontal furnaces, so they may not fit into some microfabrication facilities. However, they help to prevent dust contamination. Unlike horizontal furnaces, in which falling dust can contaminate any wafer, vertical furnaces only allow it to fall on the top wafer in the boat.

Vertical furnaces also eliminate an issue that plagued horizontal furnaces: non-uniformity of grown oxide across the wafer. Horizontal furnaces typically have convection currents inside the tube which causes the bottom of the tube to be slightly colder than the top of the tube. As the wafers lie vertically in the tube the convection and the temperature gradient with it causes the top of the wafer to have a thicker oxide than the bottom of the wafer. Vertical furnaces solve this problem by having wafer sitting horizontally, and then having the gas flow in the furnace flowing from top to bottom, significantly dampening any thermal convections.

Vertical furnaces also allow the use of load locks to purge the wafers with nitrogen before oxidation to limit the growth of native oxide on the Si surface.

Oxide quality

Wet oxidation is preferred to dry oxidation for growing thick oxides, because of the higher growth rate. However, fast oxidation leaves more dangling bonds at the silicon interface, which produce quantum states for electrons and allow current to leak along the interface. (This is called a "dirty" interface.) Wet oxidation also yields a lower-density oxide, with lower dielectric strength.

The long time required to grow a thick oxide in dry oxidation makes this process impractical. Thick oxides are usually grown with a long wet oxidation bracketed by short dry ones (a *dry-wet-dry* cycle). The beginning and ending dry oxidations produce films of high-quality oxide at the outer and inner surfaces of the oxide layer, respectively.

Mobile metal ions can degrade performance of MOSFETs (sodium is of particular concern). However, chlorine can immobilize sodium by forming sodium chloride.

Chlorine is often introduced by adding hydrogen chloride or trichloroethylene to the oxidizing medium. Its presence also increases the rate of oxidation.

Other notes

- Thermal oxidation can be performed on selected areas of a wafer, and blocked on others. Areas which are not to be oxidized are covered with a film of silicon nitride, which blocks diffusion of oxygen and water vapor. The nitride is removed after oxidation is complete. This process cannot produce sharp features, because lateral (parallel to the surface) diffusion of oxidant molecules under the nitride mask causes the oxide to protrude into the masked area.

- Because impurities dissolve differently in silicon and oxide, a growing oxide will selectively take up or reject dopants. This redistribution is governed by the segregation coefficient, which determines how strongly the oxide absorbs or rejects the dopant, and the diffusivity.

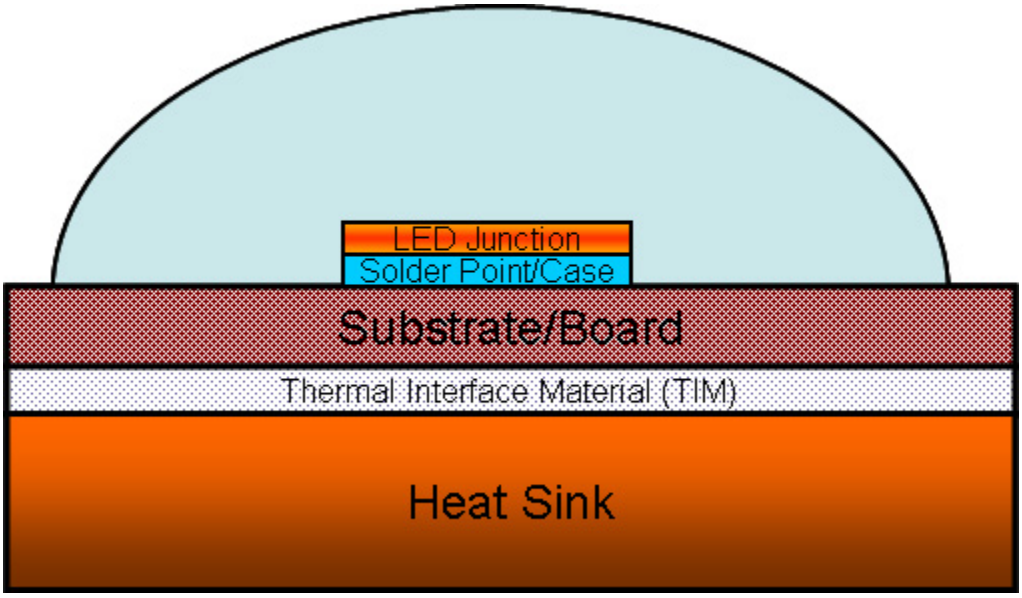
- The orientation of the silicon crystal affects oxidation. A <100> wafer oxidizes more slowly than a <111> wafer, but produces an electrically cleaner oxide interface.

- Thermal oxidation of any variety produces a higher-quality oxide, with a much cleaner interface, than chemical vapor deposition of oxide resulting in **Low Temperature Oxide** layer (reaction of TEOS at about 600 °C). However, the high temperatures required to produce High Temperature Oxide (HTO) restrict its usability. For instance, in MOSFET processes, thermal oxidation is never performed after the doping for the source and drain terminals is performed, because it would disturb the placement of the dopants.

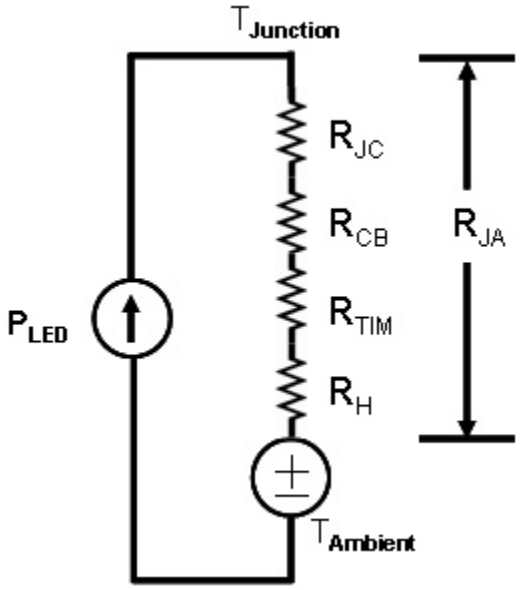
Thermal management of high-power LEDs

High power light-emitting diodes (LEDs) are likely to replace other technologies such as incandescent and fluorescent bulbs in signaling, solid state lighting, and vehicle headlights because they save energy and extend the light's lifetime. LEDs that use from 500 milliwatts to as much as 10 watts in a single package have become standard, and researchers expect to use even more power in the future. Some of the electricity in an LED becomes heat rather than light. If that heat is not removed, the LEDs run at high temperatures, which not only lowers their efficiency, but also makes the LED more dangerous and less reliable. Thus, thermal management of high power LEDs is a crucial area of research and development.

Heat transfer procedure



Typical LED package including thermal management design



Typical thermal model of LED package. LED power dissipation is modeled as a current source; thermal resistance is modeled as a resistor; and the ambient temperature is modeled as a voltage source.

In order to maintain a low junction temperature to keep good performance of an LED, every method of releasing heat from LEDs should be considered. Conduction, convection, and radiation are the three means of heat transfer. Typically, LEDs are encapsulated in a transparent resin, which is a poor thermal conductor. Nearly all heat produced is conducted through the back side of the chip. Heat is generated from the PN junction by electrical energy that was not converted to useful light, and conducted to

outside ambience through a long and extensive path, from junction to solder point, solder point to board, and board to the heat sink and then to the atmosphere. The heat path of tungsten light bulbs is almost all straight into the atmosphere, starting from filament to the glass and ending with the thermal resistance from glass to the atmosphere. A typical LED side view and its thermal model are shown in the figures.

The thermal resistance between two points is defined as the ratio of the difference in temperature to the power dissipated; the unit is ^{o}C/W. From the LED junction to the thermal contact at the bottom of package, the thermal resistance is governed by the package design. It is referred to as the thermal resistance between junction and ambient (R_{JA}). Different components in the heat conduction path can be modeled as different thermal resistances. The total power dissipated by the LED (P_{LED}) is the product of the forward voltage and the forward current of the LED, which can be modeled as a current source. The ambient temperature is modeled as a voltage source. Therefore, the junction temperature (T_J) is the sum of the ambient temperature (T_A) and the product of the thermal resistance from junction to ambient and the power dissipated. By "thermic Ohm's Law", we have the equation as follows: $T_J = T_A + (R_{JA} \times P_{LED})$, and $R_{JA} = R_{JC} + R_{CB} + R_{TIM} + R_H$

Intuitively, you can see that the junction temperature will be lower if the thermal impedance is smaller and likewise, with a lower ambient temperature. To maximize the useful ambient temperature range for a given power dissipation, the total thermal resistance from junction to ambient must be minimized. The values for the thermal resistance vary widely depending on the material or component supplier. For example, R_{JC} will range from 2.6^{o}C/W to 18^{o}C/W, depending on the LED manufacturer. The thermal interface material's (TIM) thermal resistance will also vary depending on the type of material selected. Common TIMs are epoxy, thermal grease, pressure sensitive adhesive and solder. In the most cases, power LEDs will be mounted on metal-core printed circuit boards (MCPCB), which will be attached to a heat sink. Heat flows from the LED junction through the MCPCB to the heat sink by way of conduction, and the heat sink diffuses heat to the ambient surroundings by convection. So, we can also add convection to the thermal model at the end of the heat transmission path. In the package design, the surface flatness and quality of each component, applied mounting pressure, contact area, the type of interface material and its thickness are all important parameters to thermal resistance design.

Passive thermal designs

Some considerations for passive thermal designs to ensure good thermal management for high power LED operation include:

Adhesive

Adhesive is commonly used to bond LED and board, and board and heat sinks. Using a thermal conductive adhesive can further optimize the thermal performance.

Heat sink

Heat sinks provide a path for heat from the LED source to outside medium. Heat sinks can dissipate power in three ways: conduction (heat transfer from one solid to another), convection (heat transfer from a solid to a moving fluid, for most LED applications the fluid will be air), or radiation (heat transfer from two bodies of different surface temperatures through electromagnetic waves).

- **Material** – The thermal conductivity of the material that the heat sink is made from directly affects the dissipation efficiency through conduction. Normally this is aluminum, although copper may be used with an advantage for flat-sheet heat sinks.
- **Shape** - Thermal transfer takes place at the surface of the heat sink. Therefore, heat sinks should be designed to have a large surface area. This goal can be reached by using a large number of fine fins or by increasing the size of the heat sink itself.
- **Surface Finish** - Thermal radiation of heat sinks is a function of surface finish, especially at higher temperatures. A painted surface will have a greater emissivity than a bright, unpainted one. The effect is most remarkable with flat-plate heat sinks, where about one-third of the heat is dissipated by radiation. Moreover, a perfectly flat contact area allows the use of a thinner layer of thermal compound, which will reduce the thermal resistance between the heat sink and LED source. On the other hand, anodizing or etching will also decrease the thermal resistance.
- **Mounting method**- Heat-sink mountings with screws or springs are often better than regular clips, thermal conductive glue or sticky tape.

PCB (Printed Circuit Board)

- **MCPCB** - MCPCB (Metal Core PCB) are those boards which incorporate a base metal material as heat spreader as an integral part of the circuit board. The metal core usually consists of aluminum alloy. Furthermore MCPCB can take advantage of incorporating a dielectric polymer layer with high thermal conductivity for lower thermal resistance.
- **Separation** - Separating the LED drive circuitry from the LED board prevents the heat generated by the driver from raising the LED junction temperature.

Package type

- **Flip chip** - The concept is similar to flip-chip in package configuration widely used in the silicon integrated circuit industry. Briefly speaking, the LED die is assembled face down on the sub-mount, which is usually silicon or ceramic, acting as the heat spreader and supporting substrate. The flip-chip joint can be eutectic, high-lead, lead-free solder or gold stub. The primary source of light comes from the back side of the LED chip, and there is usually a built-in reflective layer between the light emitter and the solder joints to reflect the light emitted downwards up. Several companies have adopted flip-chip packages for

their high-power LED, achieving bout 60% reduction in the thermal resistance of the LED while keeping its thermal reliability.

Chapter- 6

AAL1gator & Silicon on Insulator

AAL1gator

The **AAL1gator** is a semiconductor device that implements the Circuit Emulation Service. It was developed between 1994 and 1998 and became a run-away success. It also played a role in the acquisition of four companies. The name was based on the fact that the AAL1gator implements the ATM AAL-1 standard.

Development of the AAL1gator

The AAL1gator was developed by Network Synthesis, Inc. under contract from Integrated Telecom Technology (IgT). It was the first semiconductor solution to implement the Circuit Emulation Service standard from the ATM Forum. It implemented 8 DS1/E1 lines worth of CES and had 256 channels. It flexibly converted the PDH DS1 signal into Asynchronous Transfer Mode cells.

The AAL1gator was principally designed by the Network Synthesis CEO, Brian Holden and a consultant, Ed Lennox. Brian Holden was also involved in the ATM Forum standardization effort for the Circuit Emulation Service. Additional design efforts came from Andy Annudurai, Ravi Sajwan, and Imran Chaudhri (who also came up with the name). Chee Hu did most of the work on getting the "C" version to work at speed and to be manufacturable. Denis Smetana did most of the work on the "D" version and on the later 32 DS1 version. Jim Jacobson of OnStream Networks was the Beta Customer.

Patents on the AAL1gator

Two U.S. patents were issued on the AAL1gator's calendar-based transmit scheduler, one on the original product and an even better one on the "D" version enhancements designed by Denis Smetana . The scheduler implemented several intricate methods of minimizing the jitter caused by the scheduling of the 256 channels. The AAL1gator also could have gotten another patent on its method of queuing the SRTS samples, but the designers were too busy to get the application in.

Functions of the AAL1gator

The AAL1gator could flexibly map individual DS0s or groups of DS0s into 256 ATM VCs. It also had a high speed mode which mapped a single DS-3 into ATM. Additionally, it had a high performance implementation of the SRTS clock recovery algorithm. The original AAL1gator also was delivered along with the code for an external digital frequency synthesizer. A later version incorporated that synthesizer.

The AAL1gator has been used in several applications that were completely different than the application it was designed for. The designers knew they had a hit product when reports of these uses came in. One use was to provide fractional T1 service over microwave radio. Another use was to move DS1's around within a box.

The AAL1gator and acquisitions

The AAL1gator played a significant role in the following four technology acquisitions:

- Network Synthesis by Integrated Telecom Technology in June 1996
- Integrated Telecom Technology by PMC-Sierra in April 1998
- OnStream Networks by 3Com in 1996
- Sentient Networks by Cisco Systems in 1998

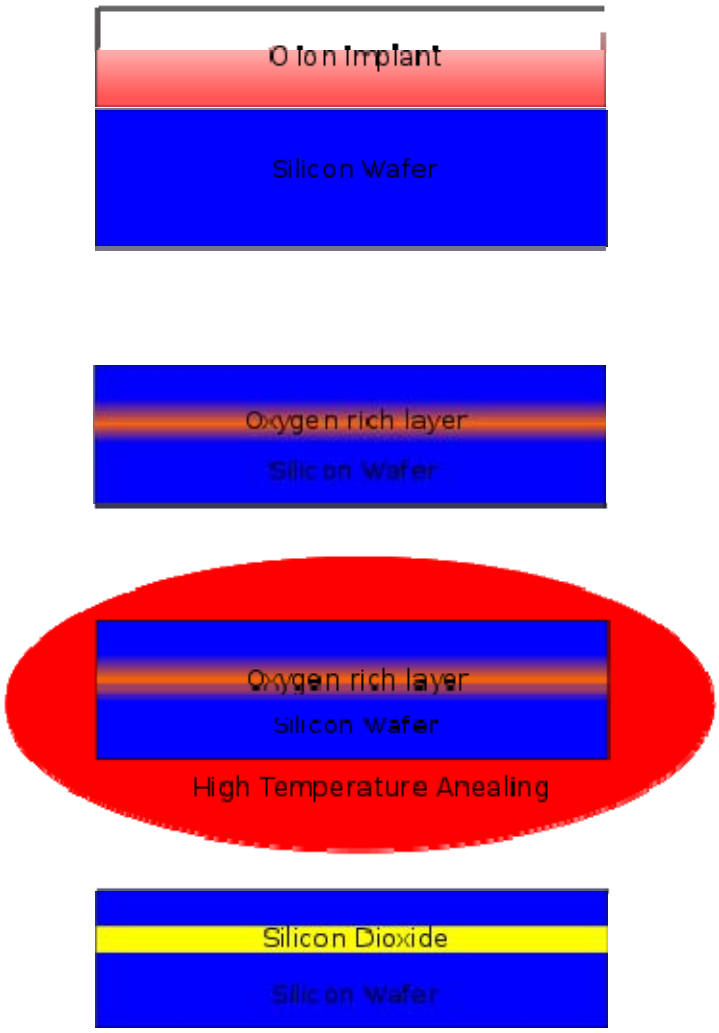
The IgT acquisition happened after the development was showing signs of success. The PMC-Sierra acquisition happened after IgT's AAL1gator began to drive the sales of T1/E1 framers from PMC-Sierra. The Onstream and Sentient acquisitions happened after successful Circuit Emulation Service (CES) product developments based on the AAL1gator.

An anecdote from the AAL1gator's development is that Brian Holden and Ed Lennox made a quick, off-handed decision in a hallway to add the "PMC Mode" to the "B" version of the device in mid-1996 to provide a glueless interface to PMC-Sierra's TQUAD and EQUAD T1 and E1 framers. Little did they know then that this off-handed decision would be a key enabler of PMC-Sierra's acquisition of the company two years later.

The AAL1gator-32

PMC-Sierra developed a 32 line version of the AAL1gator known as the AAL1gator32.

Silicon on insulator

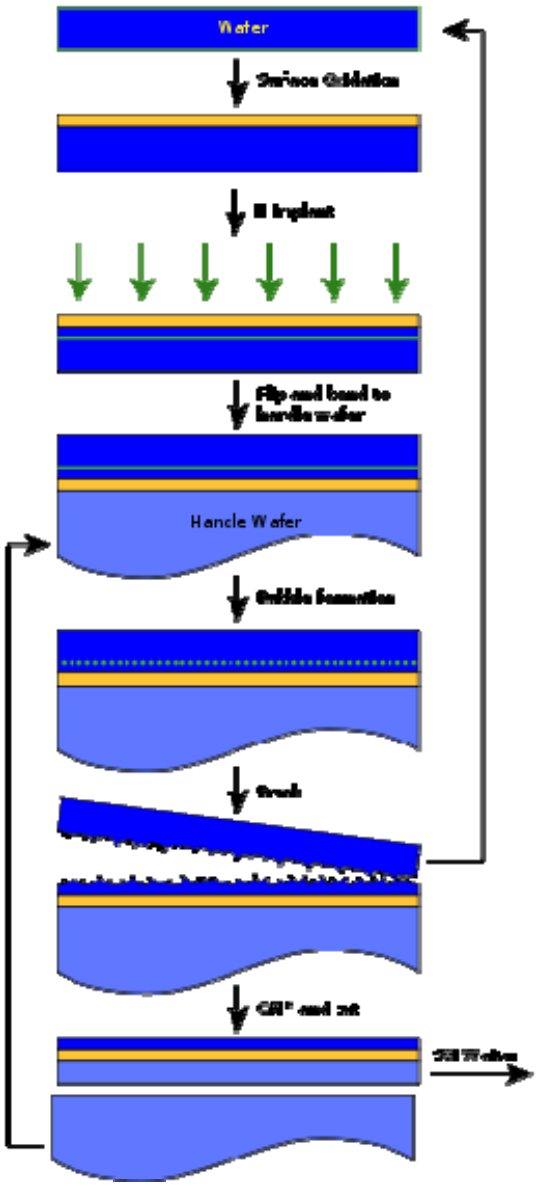


SIMOX process

Silicon on insulator technology (**SOI**) refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance and thereby improving performance. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or (less commonly) sapphire. (These types of devices are called silicon on sapphire, or SOS). The choice of insulator depends largely on intended application, with

sapphire being used for radiation-sensitive applications and silicon dioxide preferred for improved performance and diminished short channel effects in microelectronics devices . The insulating layer and topmost silicon layer also vary widely with application . The first industrial implementation of SOI was announced by IBM in August 1998.

Industry need



Smart Cut process

The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices, colloquially referred to as extending Moore's Law. Reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processing include :

- *Lower parasitic capacitance* due to isolation from the bulk silicon, which improves power consumption at matched performance.
- *Resistance to latchup* due to complete isolation of the n- and p-well structures.

From a manufacturing perspective, SOI substrates are compatible with most conventional fabrication processes. In general, an SOI-based process may be implemented without special equipment or significant retooling of an existing factory. Among challenges unique to SOI are novel metrology requirements to account for the buried oxide layer and concerns about differential stress in the topmost silicon layer. The primary barrier to SOI implementation is the drastic increase in substrate cost, which contributes an estimated 10–15% increase to total manufacturing costs.

Manufacture of SOI wafers

SiO_2-based SOI wafers can be produced by several methods:

- *SIMOX* - **S**eparation by **IM**plantation of **OX**ygen – uses an oxygen ion beam implantation process followed by high temperature annealing to create a buried SiO_2 layer.

- Wafer bonding – the insulating layer is formed by directly bonding oxidized silicon with a second substrate. The majority of the second substrate is subsequently removed, the remnants forming the topmost Si layer.
    - One prominent example of a wafer bonding process is the *Smart Cut* method developed by the French firm Soitec which uses ion implantation followed by controlled exfoliation to determine the thickness of the uppermost silicon layer.
    - *NanoCleave* is a technology developed by Silicon Genesis Corporation that separates the silicon via stress at the interface of silicon and silicon-germanium alloy.
    - *ELTRAN* is a technology developed by Canon which is based on porous silicon and water cut.
- Seed methods - wherein the topmost Si layer is grown directly on the insulator. Seed methods require some sort of template for homoepitaxy, which may be achieved by chemical treatment of the insulator, an appropriately oriented crystalline insulator, or vias through the insulator from the underlying substrate.

An exhaustive review of these various manufacturing processes may be found in reference

Use in the microelectronics industry

IBM began to use SOI in the high-end RS64-IV "Istar" PowerPC-AS microprocessor in 2000. Other examples of microprocessors built on SOI technology include AMD's 130 nm, 90 nm, 65 nm and 45 nm single, dual, quad and six core processors since 2001. Freescale adopted SOI in their PowerPC 7455 CPU in late 2001, currently Freescale is

shipping SOI products in 180 nm, 130 nm, 90 nm and 45 nm lines. The 90 nm Power Architecture based processors used in the Xbox 360, PlayStation 3 and Wii use SOI technology as well. Competitive offerings from Intel, however, such as the 65 nm Core 2 and Core 2 Duo microprocessors, are built using conventional bulk CMOS technology. Intel's new 45 nm process will continue to use conventional technology. However, Intel made a claim of single-chip silicon laser based on SOI.

On the foundry side, TSMC claimed no customer wanted SOI, but Chartered Semiconductor devoted a whole fab to SOI.

Use in Photonics

SOI wafers are widely used in silicon photonics. The crystalline silicon layer on insulator can be used to fabricate optical waveguides and other passive optical devices for integrated optics. The crystalline silicon layer in sandwiched between the buried insulator (Silicon oxide, Sapphire etc.) and top cladding of air (or Silicon oxide or any other low refractive index material). This enables propagation of electromagnetic waves in the waveguides on the basis of total internal reflection.

Chapter- 7

Applications & Examples of Semiconductor Technology

Technology aware design

Technology Aware Design (**TAD**) is a research program that started in 2001 at IMEC, Leuven, Belgium. It anticipates the end of the traditional "happy scaling" paradigm, where CMOS technology and CMOS design evolved on formally separate tracks, the interface between the two being standard cell, or SPICE compact models.

Today, both sides (design and technology) are confronted with the need to understand the other in order to overcome new scaling induced issues. The TAD program pursues analysis and solutions for these scaling induced problems.

Wafer-level optics

Wafer-level optics (WLO) enables the design and manufacture of miniaturized optics at the wafer level using advanced semiconductor-like techniques. The end product is cost effective, miniaturized optics that enable the reduced form factor of camera modules for mobile devices. . The technology is scalable from a single-element CIF/VGA lens to a multi-element mega pixel lens structure, where the lens wafers are precision aligned, bonded together and diced to form multi-element lens stacks.

LOCOS

Typical LOCOS structure.
1) Silicon 2) Silicon dioxide

LOCOS, short for **LOCal Oxidation of Silicon**, is a microfabrication process where silicon dioxide is formed in selected areas on a silicon wafer having the Si-SiO_2 interface at a lower point than the rest of the silicon surface.

This technology was developed to insulate MOS transistors from each other. The main goal is to create a silicon oxide insulating structure that penetrates under the surface of the wafer, so that the Si-SiO_2 interface occurs at a lower point than the rest of the silicon surface. This cannot be easily achieved by etching field oxide. Thermal oxidation of selected regions surrounding transistors is used instead. The oxygen penetrates in depth of the wafer, reacts with silicon and transforms it in to silicon oxide. In this way, an immersed structure is formed.

The immersed insulating barrier limits the transistor cross-talk.

Process

Typical process steps are the following:

I. Preparation of silicon substrate (layer 1)
II. CVD deposition of SiO_2, pad/buffer oxide (layer 2)
III. CVD deposition of Si_3N_4, nitride mask (layer 3)
IV. Etching of nitride layer (layer 3) and silicon oxide layer (layer 2)
V. Thermal growth of silicon oxide (structure 4)
VI. Further growth of thermal silicon oxide (structure 4)
VII. Removal of nitride mask (layer 3)

There are 4 basic layers/structures:

1. Si, silicon substrate, wafer
2. SiO_2, buffer oxide (pad oxide), chemical vapor deposition silicon oxide
3. Si_3N_4, nitride mask
4. SiO_2, insulation oxide, thermal o

Function of layers and structures

The silicon wafer (layer 1) is used as a basis for building electronic structures (such as MOS transistors).

To perform local oxidation, the areas not meant to be oxidized will be coated in a material that does not permit the diffusion of oxygen at high temperatures (thermal oxidation is performed in temperatures between 800 and 1200°C), such as silicon nitride (layer 3, step III).

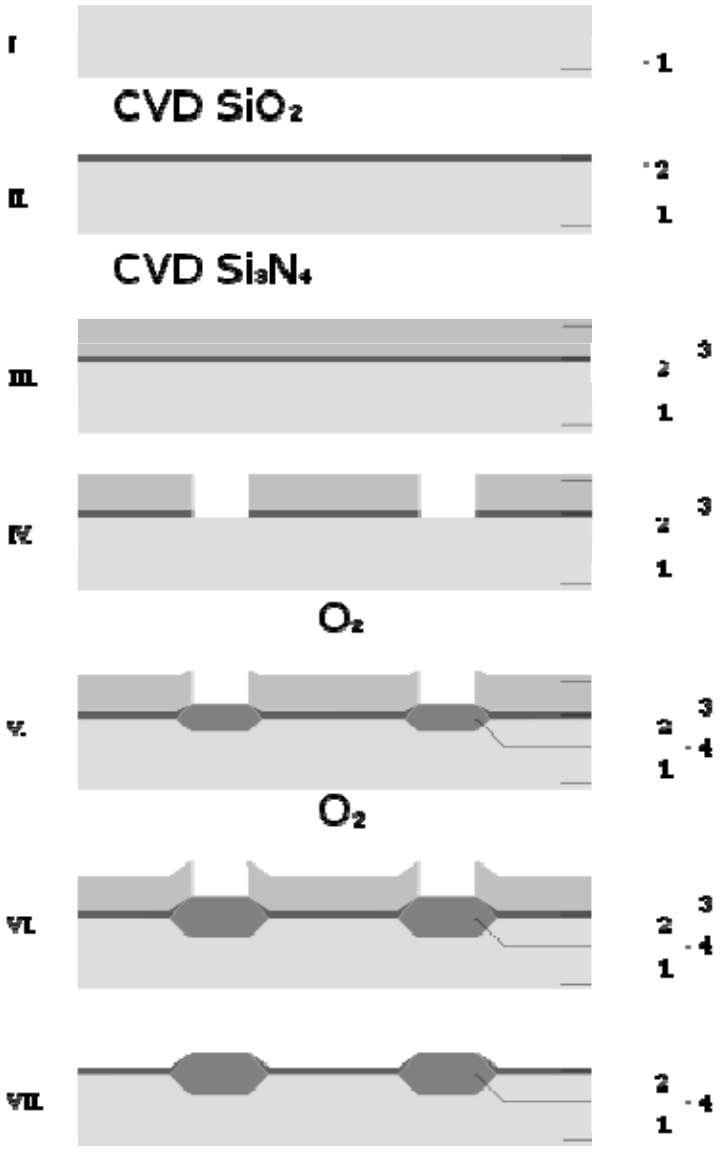
During the growth of the immersed insulating thermal oxide structures (steps V and VI), the silicon nitride layer (layer 3) is pushed upwards. Without the buffer oxide (layer 2, also known as pad oxide), this would create too much tension in the Si substrate (layer 1), the plastic deformation would occur and the electronic devices would be damaged.

Therefore a buffer oxide (layer 2) is deposed by the CVD (step II) between the Si substrate (layer 1) and the silicon nitride (layer 3). At high temperatures, the viscosity of silicon oxide decreases and the stress created between the silicon substrate (layer 1) and nitride layer (layer 3), by the growth of the thermal oxide (steps V and VI), is relieved.

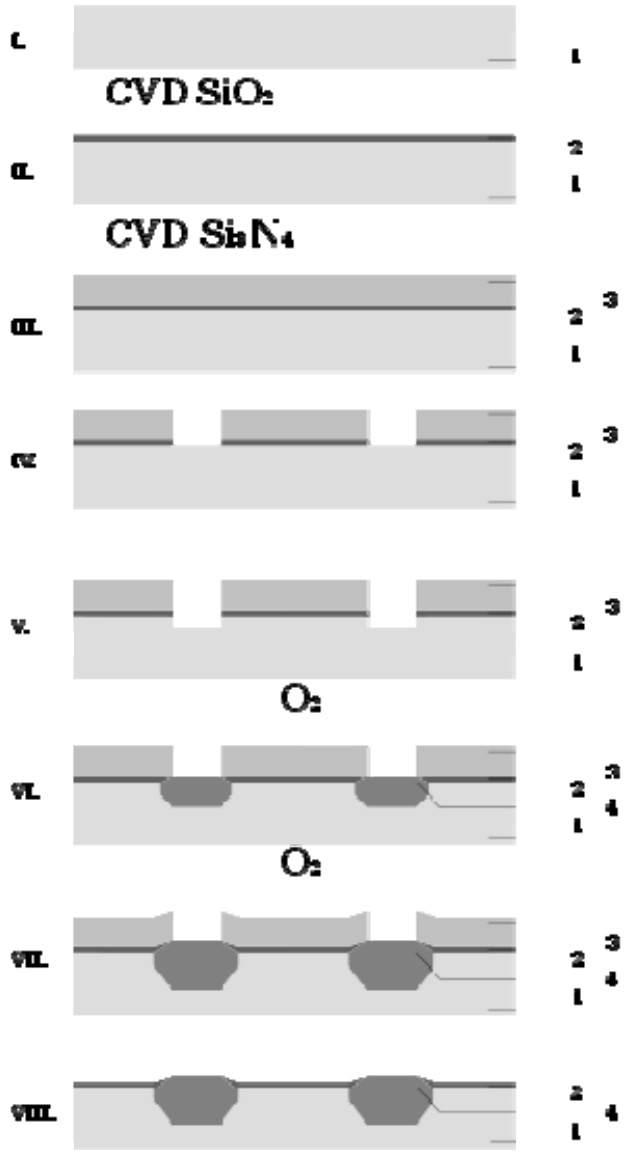
The insulating structures (structure 4) are formed by thermal oxidation of silicon. During this process, the silicon wafer is "consumed" and "replaced" by silicon oxide. The volume of silicon oxide to silicon is about 2.4:1, which explains the growth of the insulation structures and the created tension.

The disadvantage of this technology is that the insulating structures are rather large, and therefore, less MOS transistors can be formed on one wafer.

Reduction of dimensions of insulating structures is solved by the STI (Shallow Trench Isolation, also known as Box Isolation Technique). In this process, trenches are formed and silicon dioxide is deposed inside. The LOCOS technology can't be used in this way, because of the change of the volume during the thermal oxidation, which would induce too much stress in the trenches.



LOCOS process steps:
I. Preparation of silicon substrate
II. CVD deposition of SiO_2, pad/buffer oxide
III. CVD deposition of Si_3N_4, nitride mask
IV. Etching of nitride layer and silicon oxide layer
V. Thermal growth of silicon oxide
VI. Further growth of thermal silicon oxide
VII. Removal of nitride mask
LOCOS process materials:
1) Si, silicon substrate
2) SiO_2, pad/buffer oxide, chemical vapor deposition silicon oxide
3) Si_3N_4, nitride mask
4) SiO_2, isolation oxide, thermal oxide



Fully recessed LOCOS structure process steps:
I. Preparation of silicon substrate
II. CVD deposition of SiO_2, pad/buffer oxide
III. CVD deposition of Si_3N_4, nitride mask
IV. Etching of nitride layer and silicon oxide layer
V. Silicon etching
VI. Thermal growth of silicon oxide
VII. Further growth of thermal silicon oxide
VIII. Removal of nitride mask

Optical beam-induced currents

Optical Beam-Induced Current (**OBIC**) is a semiconductor analysis technique that employs a scanning laser beam to induce a current flow within a semiconductor sample which may be collected and analyzed to generate images that represent the sample's properties. It is a useful imaging technique for detecting or locating various defects or anomalies on a semiconductor sample. Conventional OBIC scans an ultrafast laser beam over the surface of the sample, exciting some electrons into the conduction band through what is known as 'single-photon absorption'. As its name implies, single-photon absorption involves just a single photon to excite the electron into conduction. This can only occur if that single photon carries enough energy to overcome the band gap of the semiconductor (1.2 eV for Si) and provide the electron with enough energy to make it jump into the conduction band.

Proximity communication

Proximity communication is a Sun microsystems technology of wireless chip-to-chip communications. Partly by Robert Drost and Ivan Sutherland. Research done as part of High Productivity Computing Systems DARPA project.

Proximity communication replaces wires by capacitive coupling, promises significant increase in communications speed between chips in an electronic system, among other benefits. Partially funded by a $50 million award from the Defense Advanced Research Projects Agency.

Comparing traditional area ball bonding, proximity communication has one order smaller scale, so it can be two order densier (in terms of connection number/pin number) than ball bonding. This technique require very good alignment between chips and very small gaps between tx and rx parts (2-3 micrometers), which can be destroyed by thermal expansion, vibration, dust, etc.

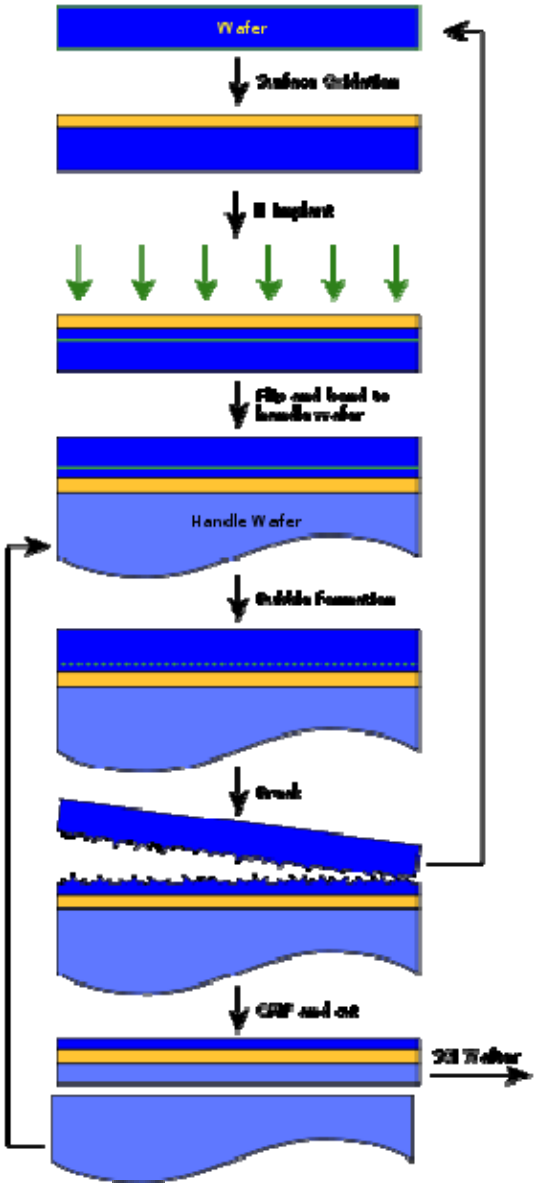
Chip transmitter consists (according to presentation slide) of big 32x32 array of very small Tx micropads, 4x4 array of bigger Rx micropads (four times bigger than tx micropad), and two linear arrays of 14 X vernier and 14 Y vernier.

Proximity communication can be used with 3D packing on chips in Multi-Chip Module, allowing to connect several MCM without sockets and wires.

Speed was up to 1.35 Gbps/channel in tests of 16 channel systems. BER < 10^{-12}. Static power is 3.6 mW/channel, dynamic power is 3.9 pJ/bit

Current status of the project is unknown.

Smart Cut



Smart Cut process

Smart Cut is a technological process that enables the transfer of very fine layers of crystalline material onto a mechanical support. The application of this technological procedure is used mainly in silicon-on-insulator (SOI). The role of SOI is to electronically insulate a fine layer of monocrystalline silicon from the rest of the silicon wafer; an ultra-thin silicon film is transferred to a mechanical support, thereby introducing an intermediate, insulating layer. Semiconductor manufacturers can then

fabricate integrated circuits on the top layer of the SOI wafers using the same processes they would use on plain silicon wafers. The wafers are then cut up and the chips packaged for mounting on the cards that are integrated into electronic systems such as personal computers. The Smart Cut process was developed and is patented by SOITEC corporation from France.

Chapter- 8

Semiconductor Technology Material

Aluminium nitride

Aluminium nitride (AlN) is a nitride of aluminium. Its wurtzite phase (w-AlN) is a wide band gap (6.2 eV) semiconductor material, giving it potential application for deep ultraviolet optoelectronics.

History

AlN was first synthesized in 1877, but it was not until the middle of the 1980s that its potential for application in microelectronics was realized due to its relative high thermal conductivity for an electrical insulating ceramic (70–210 $W \cdot m^{-1} \cdot K^{-1}$ for polycrystalline material, and as high as 285 $W \cdot m^{-1} \cdot K^{-1}$ for single crystals).

Stability and chemical properties

Aluminium nitride is stable at high temperatures in inert atmospheres and melts at 2800 °C. In a vacuum, AlN decomposes at ~1800 °C. In the air, surface oxidation occurs above 700°C, and even at room temperature, surface oxide layers of 5-10 nm have been detected. This oxide layer protects the material up to 1370°C. Above this temperature bulk oxidation occurs. Aluminium nitride is stable in hydrogen and carbon dioxide atmospheres up to 980°C.

The material dissolves slowly in mineral acids through grain boundary attack, and in strong alkalies through attack on the aluminium nitride grains. The material hydrolyzes slowly in water. Aluminium nitride is resistant to attack from most molten salts, including chlorides and cryolite.

Manufacture

AlN is synthesized by the carbothermal reduction of alumina or by direct nitridation of aluminium. The use of sintering aids and hot pressing is required to produce a dense technical grade material.

Applications

Metallization methods are available to allow AlN to be used in electronics applications similar to those of alumina and beryllium oxide.

Currently there is much research into developing light-emitting diodes to operate in the ultraviolet using the gallium nitride based semiconductors and, using the alloy aluminum gallium nitride, wavelengths as short as 250 nm have been achieved. In May 2006, an inefficient AlN LED emission at 210 nm has been reported.

Among the applications of AlN are

- opto-electronics,
- dielectric layers in optical storage media,
- electronic substrates, chip carriers where high thermal conductivity is essential,
- military applications,
- as a crucible to grow crystals of gallium arsenide,
- steel and semiconductor manufacturing.

Epitaxially grown thin film crystalline aluminium nitride is also used for surface acoustic wave sensors (SAW's) deposited on silicon wafers because of the AlN's piezoelectric properties. One application is an RF filter used in mobile phones called a thin film bulk acoustic resonator (FBAR). This is a MEMS device that uses aluminium nitride sandwiched between two metal layers.

Aluminium phosphide

Aluminium phosphide is the chemical compound with the empirical formula AlP. This colourless solid is generally sold as a grey-green-yellow powder due to the presence of impurities arising from hydrolysis and oxidation. This material is a wide band gap semiconductor and is used as a fumigant.

Structure, synthesis, and chemical properties

AlP crystallizes in the cubic zinc blende lattice, wherein all atoms have tetrahedral coordination. Related materials crystallize similarly, including GaAs. At pressures of 14-17 GPa, AlP transforms into a rocksalt phase .

Crude aluminium phosphide can be prepared in the laboratory by igniting a mixture of red phosphorus and powdered aluminium.

Aluminium phosphide reacts with water or acids to release phosphine.

$$AlP + 3\ H_2O \rightarrow Al(OH)_3 + PH_3$$
$$AlP + 3\ H^+ \rightarrow Al^{3+} + PH_3$$

Physical properties

Aluminium phosphide has a hardness of 5.5 on the Mohs scale .

Pesticide

AlP is used as a rodenticide, insecticide, and fumigant for stored cereal grains. It is used to kill small verminous mammals such as moles, rabbits, and rodents. The tablets or pellets typically also contain other chemicals that evolve ammonia which helps to reduce the potential for spontaneous ignition or explosion of the phosphine gas.

As a rodenticide, aluminium phosphide pellets are provided as a mixture with food for consumption by the rodents. The acid in the digestive system of the rodent reacts with the phosphide to generate the toxic phosphine gas. Other pesticides similar to aluminium phosphide are zinc phosphide and calcium phosphide.

As a rodenticide, aluminium phosphide can be encountered under various brand names, e.g. **Celphos**, **Fumitoxin**, **Phostoxin**, and **Quick Phos**.

Evidently poisonous, aluminium phosphide has been used for suicide. Fumigation has also caused unintentional deaths, such as examples in Saudi Arabia and the United States. Known as "rice tablet" in Iran, for its use to preserve rice, there have been frequent incidents of accidental or intentional death. There is a campaign by Iranian Forensic Medicine Organization to stop its use as a pesticide.

Semiconductor applications

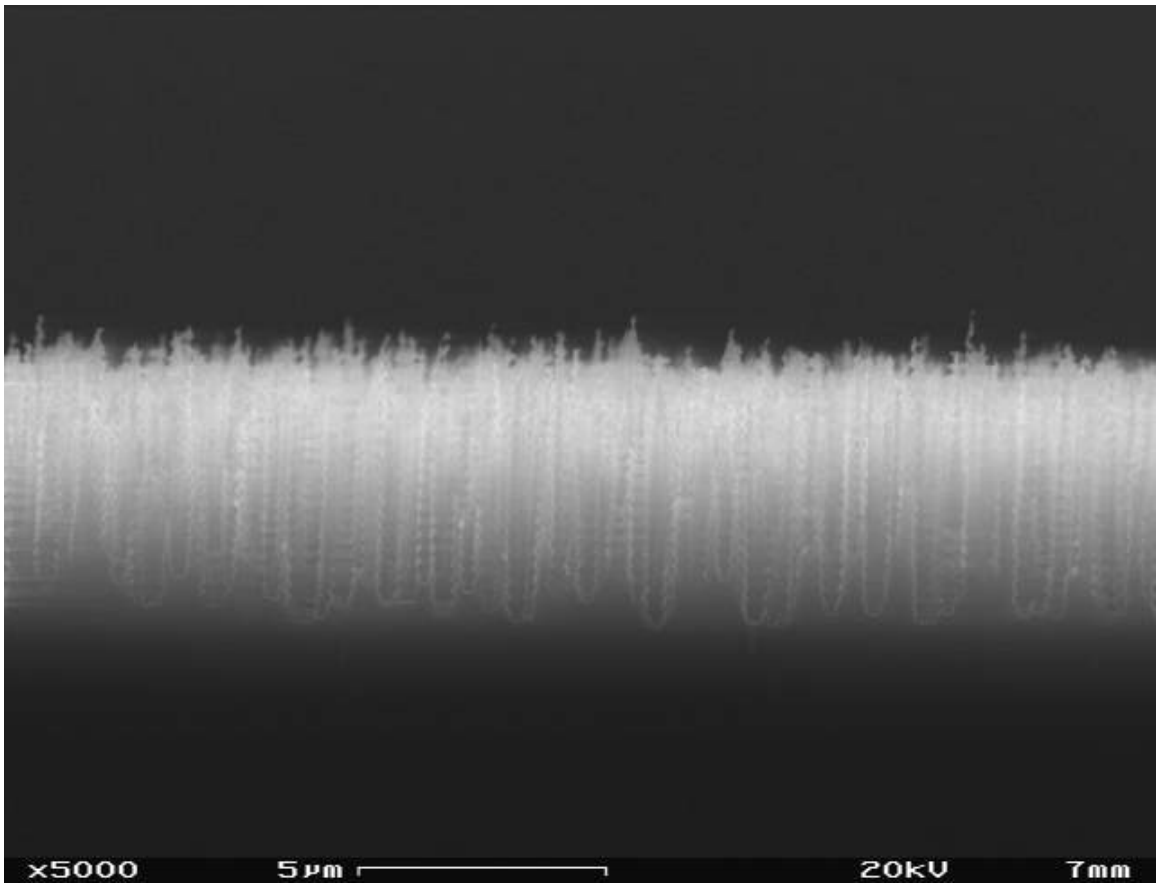
Industrially, AlP is a semiconductor material that is usually alloyed with other binary materials for applications in devices such as light-emitting diodes (e.g. aluminium gallium indium phosphide).

Black silicon

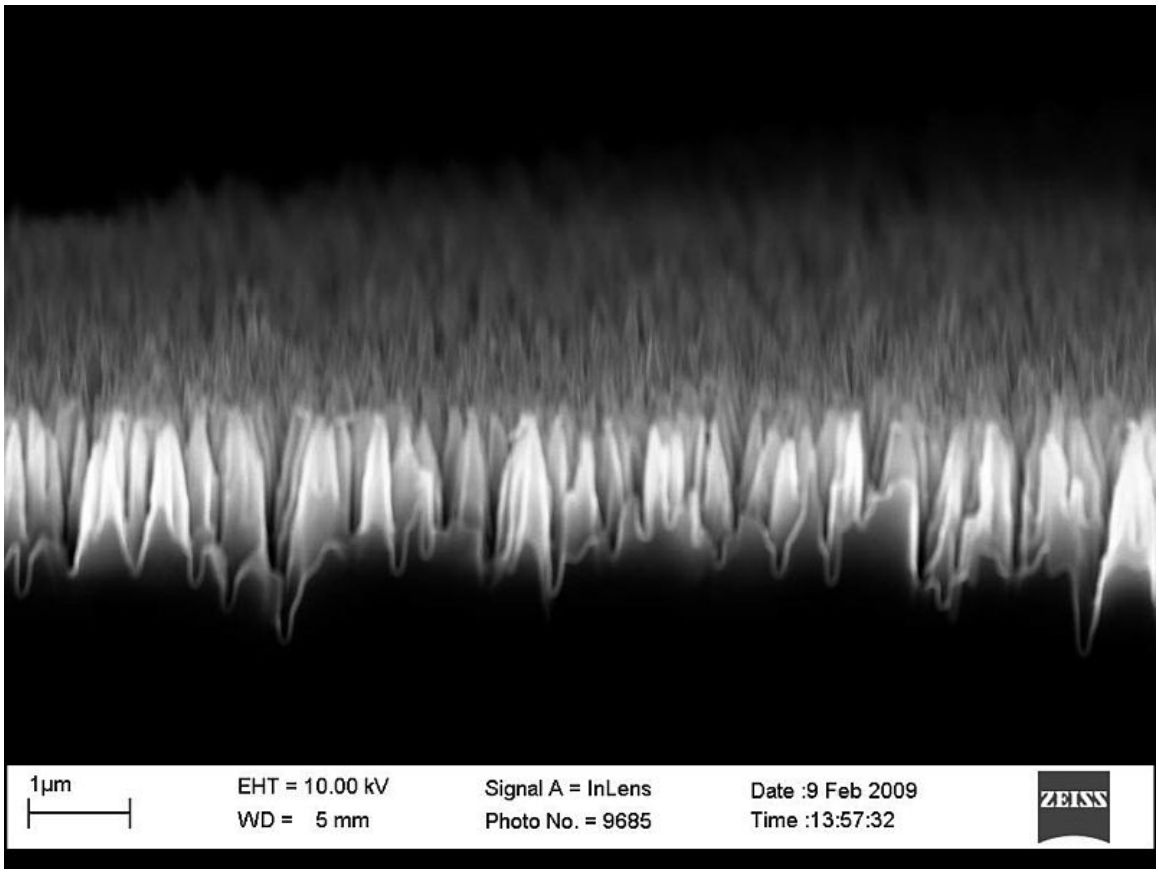
Black silicon is a semiconductor material, a surface modification of silicon with very low reflectivity and correspondingly high absorption of visible (and infrared) light. The modification was discovered in the 1980s as an unwanted side effect of reactive ion

etching (RIE). Another method for forming a similar structure was developed in Eric Mazur's laboratory at Harvard University (1998).

Properties



Scanning electron micrograph of black silicon, produced by RIE (ASE process)



SEM micrograph of black silicon formed by cryogenic RIE. Notice the smooth, sloped surfaces, unlike the undulated sidewalls obtained with the Bosch process RIE.

Black silicon is a needle-shaped surface structure where needles are made of single-crystalline silicon and have a height above 10 microns and diameter <1 micron. Its main feature is an increased absorption of incident light – the high reflectivity of the silicon, which is usually 20–30% for quasi-normal incidence, is reduced to about 5%. This is due to the formation of a so-called effective medium by the needles. Within this medium, there is no sharp interface, but a continuous change of the refractive index that reduces Fresnel reflection.

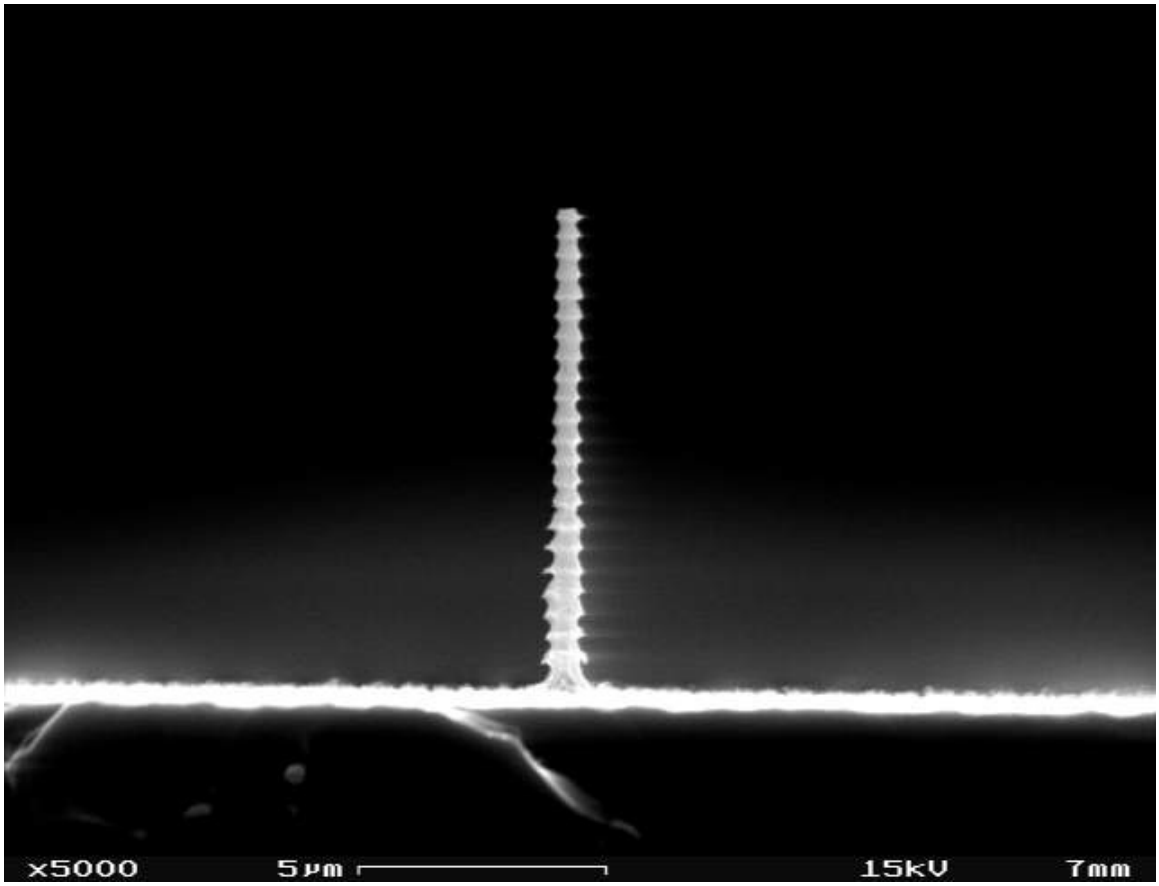
Applications

The unusual optical characteristics, combined with the semiconducting properties of silicon make this material interesting for sensor applications. The potential applications include:

- Image sensors with increased sensitivity
- Thermal imaging cameras
- Photodetector with high efficiency through increased absorption.
- Mechanical contacts and interfaces
- Terahertz applications.

- Solar Cells

Production by RIE



Scanning electron micrograph of a single "needle" of black silicon, produced by RIE (ASE process)

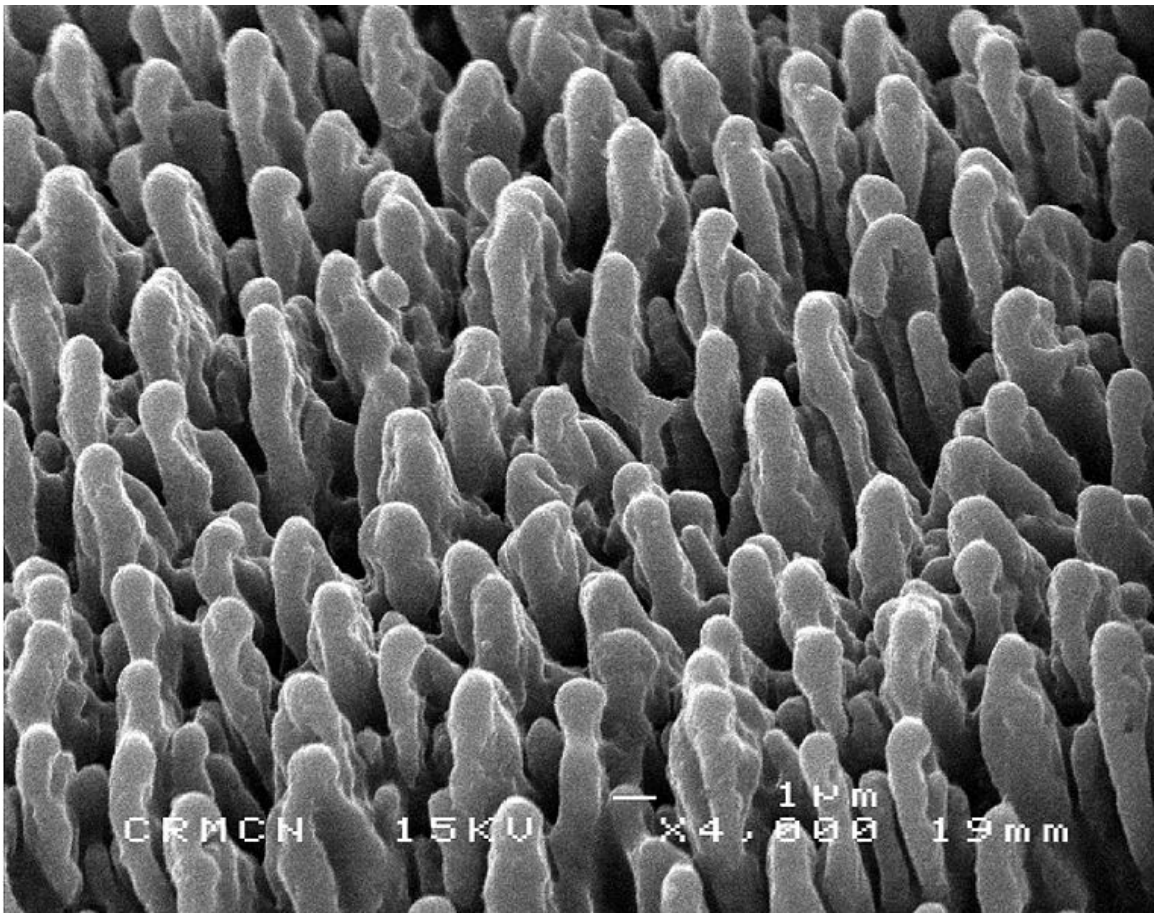
In semiconductor technology, RIE is a standard procedure for the producing trenches and holes with a depth of up to several hundred microns and very high aspect ratios. In Bosch process RIE, this is achieved by repeatedly switching between an etching and passivation. With cryogenic RIE, the low temperature and oxygen gas achieve this sidewall passivation by forming SiO_2, easily removed from the bottom by directional ions. Both RIE methods can produce black silicon, but the morphology of the resulting structure differs substantially. The switching between etching and passivation of the Bosch process creates undulated sidewalls, which are visible also on the black silicon formed this way.

During etching, however, small debris remain on the substrate; they mask the ion beam and produce structures that are not removed and in the following etching steps and result in tall silicon pillars. The process can be set so that a million needles are formed on an area of one square millimeter.

Production by Mazur's method

Material

In 1999, a group led by Eric Mazur and James Carey at the Harvard University developed a process in which black silicon was produced by irradiating silicon with femtosecond laser pulses. After irradiation in the presence of a gas containing sulfur hexafluoride and other dopants, the surface of silicon develops a self-organized microscopic structure of micrometer-sized cones. The resulting material has many remarkable properties, such as an enhanced absorption that extends to the infrared below the band gap of silicon, including the wavelengths for which unmodified silicon is transparent. This property is caused by sulfur atoms being forced to the silicon surface, creating a structure with a lower band gap and therefore the ability to absorb longer wavelengths.



Black silicon made without special gas ambient - laboratory LP3-CNRS

Similar surface modification can be achieved in vacuum using the same type of laser and laser processing conditions. In this case, the individual silicon micro-cones are lack of sharp tip but more in a penguin-like form. The reflectivity of such a micro-structured surface is very low, 3~14% in the spectral range 350–1150 nm. Such reduction in reflectivity is considered to be contributed by the geometry of these micro-cones, which

increases the light internal reflections between themselves and hence the possibility of light absorption by the silicon is increased. The gain in absorption achieved by fs laser texturization is found to be superior to that achieved by using alkaline chemical etch method, which is a standard industrial approach for surface texturization of mono-crystalline silicon wafers in solar cell manufacturing. It is also found that such surface modification is independent to local crystalline orientation. Uniform texturisation effect can be achieved across the whole surface of a multi-crystalline silicon wafer. These findings make it an attractive potential alternative to chemical surface texturisation process in solar cell manufacturing.

Function

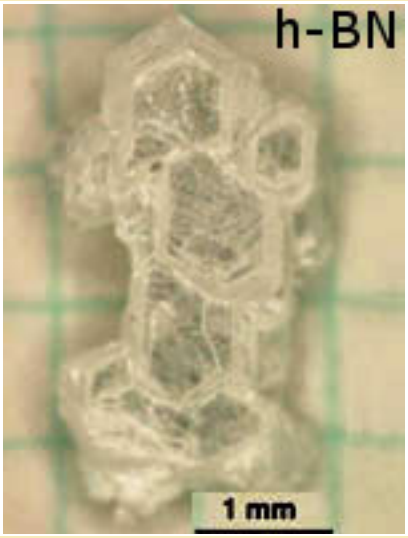
When the material is biased by a small electric voltage, absorbed photons are able to excite dozens of electrons. The sensitivity of black silicon detectors is 100–500 times higher than that of untreated silicon (conventional silicon), in both the visible and infrared spectra.

Uses and commercialization

The material has found commercial applications in a number of photodetectors for various imaging and night vision applications. Black silicon is currently being commercialized by SiOnyx, a Massachusetts-based venture-funded startup company which acquired licensing for the process from Harvard in 2006.

Black silicon also has potential application for high efficiency solar cells, which is being explored by Solasys, an EU Seventh Framework Programme funded demonstration project aiming at lowering manufacturing costs while increasing cell efficiency at the same time.

Boron nitride

Boron nitride


Identifiers	
CAS number	10043-11-5
PubChem	66227
ChemSpider	59612
EC number	233-136-6
RTECS number	ED7800000
SMILES	
InChI	

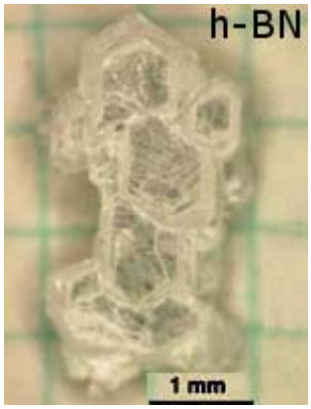
Properties	
Molecular formula	BN
Molar mass	24.818 g/mol
Appearance	white powder or translucent crystals (both c-BN and h-BN)
Density	3.4870 g/cm^3 (cBN)
Melting point	2973 °C (cBN) (sublimes)
Solubility in water	insoluble
Solubility	insoluble in acids
Electron mobility	200 cm^2/(V·s) (cBN)
Refractive index (n_D)	2.17 (cBN)

Structure	
Crystal structure	hexagonal, sphalerite, wurtzite

Thermochemistry	
Std enthalpy of	476.98 kJ mol^{-1}

formation $\Delta_f H^\circ_{298}$	
Std enthalpy of combustion $\Delta_c H^\circ_{298}$	−250.91 kJ mol^{-1}
Standard molar entropy S°_{298}	14.77 J mol^{-1} K^{-1}
Hazards	
R-phrases	R36, R37
S-phrases	S26, S36
Related compounds	
Other anions	BP, BAs B_4C, B_2O_3

Boron nitride is a chemical compound with chemical formula BN, consisting of equal numbers of boron and nitrogen atoms. BN is isoelectronic to a similarly structured carbon lattice and thus exists in various crystalline forms. The hexagonal form corresponding to graphite is the most stable and softest among BN polymorphs, and is therefore used as a lubricant and an additive to cosmetic products. The cubic (sphalerite structure) variety analogous to diamond is called c-BN. Its hardness is inferior only to diamond, but its thermal and chemical stability is superior. The rare wurtzite BN modification is similar to lonsdaleite and may even be harder than the cubic form.



Boron nitride is not found in nature and is therefore produced synthetically from boric acid or boron trioxide. The initial product is amorphous BN powder, which is converted to crystalline h-BN by heating in nitrogen flow at temperatures above 1500 °C. c-BN is made by annealing h-BN powder at higher temperatures, under pressures above 5 GPa. Contrary to diamond, larger c-BN pellets can be produced by fusing (sintering) relatively cheap c-BN powders. As a result, c-BN is widely used in mechanical applications.

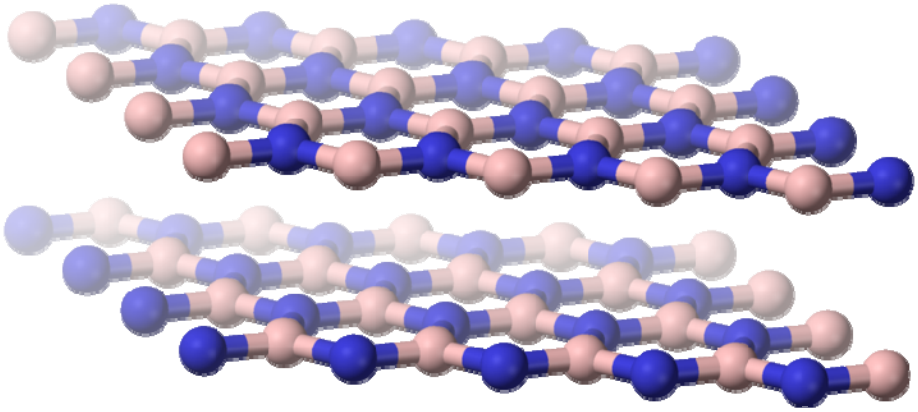
Because of excellent thermal and chemical stability, boron nitride ceramics are traditionally used as parts of high-temperature equipment. Boron nitride has a great potential in nanotechnology. Nanotubes of BN can be produced that have a structure similar to that of carbon nanotubes, i.e. graphene (or BN) sheets rolled on themselves,

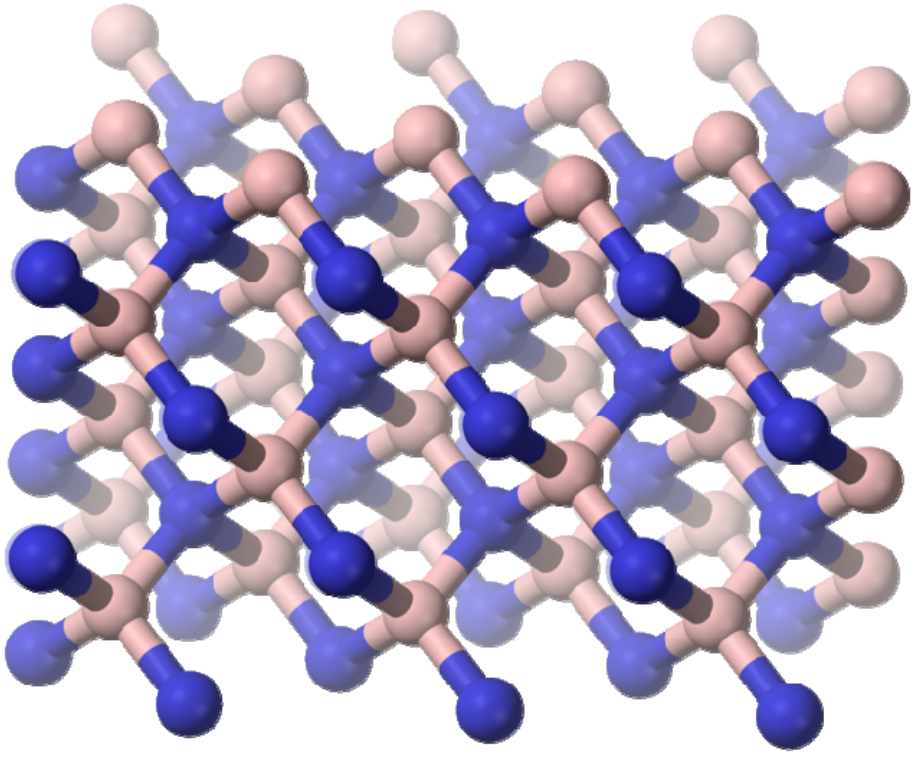
however the properties are very different: whereas carbon nanotubes can be metallic or semiconducting depending on the rolling direction and radius, a BN nanotube is an electrical insulator with a wide bandgap of ~5.5 eV (same as in diamond), which is almost independent of tube chirality and morphology. Similar to other BN forms, BN nanotubes are more thermally and chemically stable than carbon nanotubes which favors them for some applications.

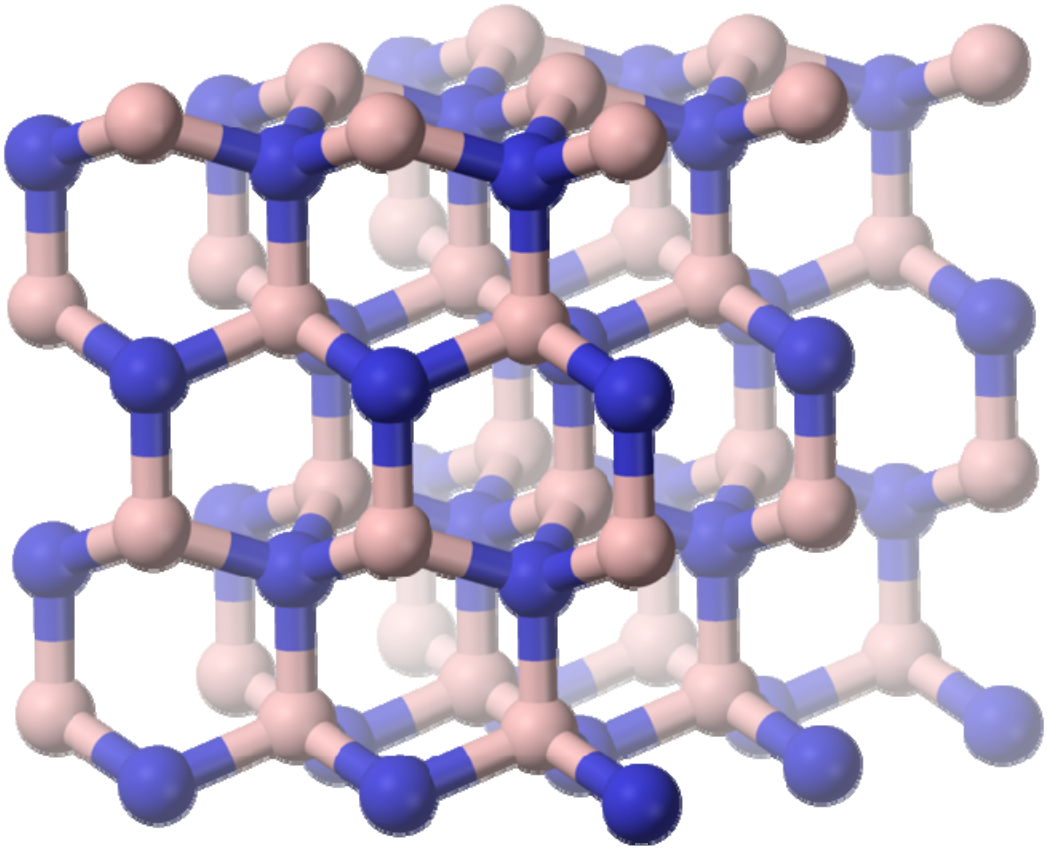
Structure

Boron nitride has been produced in an amorphous (a-BN) and crystalline forms. The most stable crystalline form is the hexagonal one, also called h-BN, α-BN, or g-BN (graphitic BN). It has a layered structure similar to graphite. Within each layer, boron and nitrogen atoms are bound by strong covalent bonds, whereas the layers are held together by weak van der Waals forces. The interlayer "registry" of these sheets differs, however, from the pattern seen for graphite, because the atoms are eclipsed, with boron atoms lying over and above nitrogen atoms. This registry reflects the polarity of the B-N bonds. Still, h-BN and graphite are very close neighbors and even the BC_6N hybrids have been synthesized where carbon substitutes for some B and N atoms.

As diamond is less stable than graphite, cubic BN is less stable than h-BN, but the conversion rate between those forms is negligible at room temperature. The cubic form has the sphalerite crystal structure, same as diamond structure, and is also called β-BN or c-BN. The wurtzite BN form (w-BN) has similar structure as lonsdaleite, rare hexagonal polymorph of carbon. In both c-BN and w-BN boron and nitrogen atoms are grouped into tetrahedra, but the angles between neighboring tetrahedra are different.







α-BN, hexagonal
β-BN, sphalerite structure
BN, wurtzite structure

Properties

Physical

Properties of amorphous and crystalline BN, graphite and diamond.
Some properties of h-BN and graphite differ within the basal planes (∥) and perpendicular to them (⊥)

Material	a-BN	h-BN	c-BN	w-BN	graphite	diamond
Density (g/cm^3)	2.28	~2.1	3.45	3.49	~2.1	3.515
Mohs hardness		1-2	~10	~10	1-2	10
Knoop hardness (GPa)	10		45	34		100
Bulk modulus	100	36.5	400	400	34	440

(GPa)						
Thermal conductivity (W/cm K)	0.03	6∥; 0.3⊥	7.4		2-20∥; 0.02-0.8⊥	6-20
Thermal expansion (10^{-6}/°C)		-2.7∥; 38⊥	1.2	2.7	-1.5∥; 25⊥	0.8
Bandgap (eV)	5.05	5.2	6.4	4.5-5.5	0	5.5
Refractive index	1.7	1.8	2.1	2.05		2.4
Magnetic susceptibility (μemu/g)		-0.48∥; -17.3⊥			-0.2..-2.7∥; -20..-28⊥	-1.6

Sources: amorphous BN, crystalline BN, graphite, diamond.

The partly ionic structure of BN layers in h-BN reduces covalency and electrical conductivity, whereas the interlayer interaction increases resulting in higher hardness of h-BN relative to graphite. The reduced electron-delocalization in hexagonal-BN is also indicated by its absence of color and a large band gap. Very different bonding - strong covalent within the basal planes (planes where boron and nitrogen atoms are covalently bonded) and weak between them - causes high anisotropy of most properties of h-BN.

For example, the hardness, electrical and thermal conductivity are much higher within the planes than perpendicular to them. On the contrary, the properties of c-BN and w-BN are more homogeneous.

Those materials are extremely hard, with the hardness of c-BN being slightly smaller and w-BN even higher than that of diamond. Because of much better stability to heat and metals, c-BN surpasses diamond in mechanical applications. The thermal conductivity of BN is among the highest of all electric insulators (see table).

Boron nitride can be doped p-type with Be and n-type with boron, sulfur, silicon or if co-doped with carbon and nitrogen. Both hexagonal and cubic BN are wide-gap semiconductors with a band gap energy corresponding to the UV region. If voltage is applied to h-BN or c-BN, then it emits UV light in the range 215-250 nm and therefore can potentially be used as light emitting diodes (LEDs) or lasers.

Little is known on melting behavior of boron nitride. It sublimates at 2973 °C at normal pressure releasing nitrogen gas and boron, but melts at elevated pressure.

Thermal stability

Hexagonal and cubic (and probably w-BN) BN show remarkable chemical and thermal stabilities. For example, h-BN is stable to decomposition in temperatures up to 1000 °C in air, 1400 °C in vacuum, and 2800 °C in an inert atmosphere. The reactivity of h-BN and c-BN is relatively similar, and the data for c-BN are summarized in the table below.

Reactivity of c-BN with solids			
Solid	**Ambient**	**Action**	**Threshold T (°C)**
Mo	10^{-2} Pa vacuum	reaction	1360
Ni	10^{-2} Pa vacuum	wetting	1360
Fe, Ni, Co	argon	react	1400–1500
Al	10^{-2} Pa vacuum	wetting and reaction	1050
Si	10^{-3} Pa vacuum	wetting	1500
Cu, Ag, Au, Ga, In, Ge, Sn	10^{-3} Pa vacuum	no wetting	1100
B		no wetting	2200
$Al_2O_3 + B_2O_3$	10^{-2} Pa vacuum	no reaction	1360

Thermal stability of c-BN can be summarized as follows:

- In air or oxygen: B_2O_3 protective layer prevents further oxidation to ~1300 °C; no conversion to hexagonal form at 1400 °C.
- In nitrogen: some conversion to h-BN at 1525 °C after 12 h.
- In vacuum (10^{-5} Pa): conversion to h-BN at 1550 - 1600 °C.

Chemical stability

Boron nitride is insoluble in usual acids, but is soluble in alkaline molten salts and nitrides, such as LiOH, KOH, NaOH-Na_2CO_3, $NaNO_3$, Li_3N, Mg_3N_2, Sr_3N_2, Ba_3N_2 or Li_3BN_2, which are therefore used to etch BN.

Thermal conductivity

The theoretical thermal conductivity of hexagonal Boron nitride nanoribbons (BNNRs) can approach 1700-2000 W/(m·K), which has the same order of magnitude as the experimental measured value for graphene, and can be comparable to the theoretical calculations for graphene nanoribbons. Moreover, the thermal transport in the BNNRs is anisotropic. The thermal conductivity of zigzag-edged BNNRs is about 20% larger than that of armchair-edged nanoribbons at room temperature.

Synthesis

Boron nitride has not been found in nature and therefore is produced synthetically. The most common raw materials for BN synthesis, boric acid and boron trioxide are produced on industrial scales by treating minerals borax and colemanite with sulfuric acid or hydrochloric acid:

$$Na_2B_4O_7{\cdot}10H_2O \text{ (borax)} + H_2SO_4 \rightarrow 4\ H_3BO_3 \text{ (boric acid)} + Na_2SO_4 + 5\ H_2O$$

Boron trioxide is obtained by heating boric acid.

Preparation and reactivity of hexagonal BN

Hexagonal boron nitride is obtained by the reacting boron trioxide (B_2O_3) or boric acid ($B(OH)_3$) with ammonia (NH_3) or urea ($CO(NH_2)_2$) in nitrogen atmosphere:

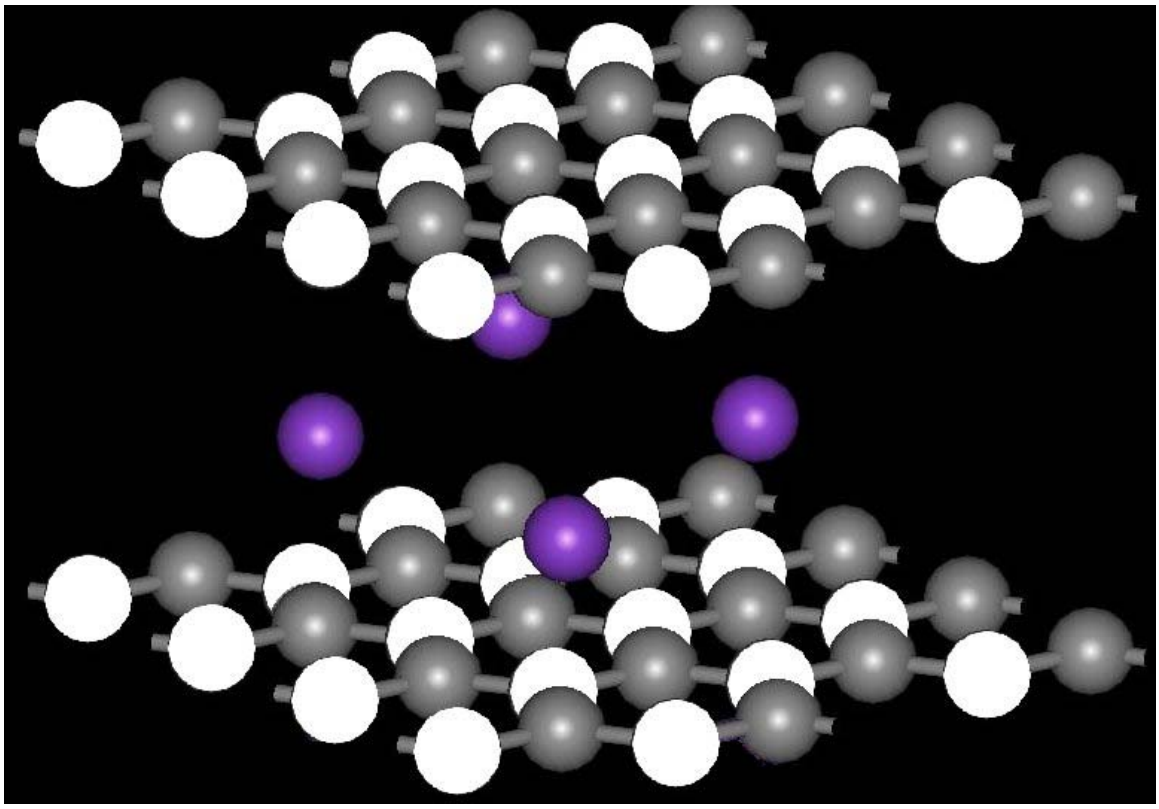
$$B_2O_3 + 2\ NH_3 \rightarrow 2\ BN + 3\ H_2O \text{ (T = 900 °C)}$$
$$B(OH)_3 + 3\ NH_3 \rightarrow BN + 2\ NH_3 + 3\ H_2O \text{ (T = 900 °C)}$$
$$B_2O_3 + CO(NH_2)_2 \rightarrow 2\ BN + CO_2 + 2\ H_2O \text{ (T > 1000 °C)}$$
$$B_2O_3 + 3\ CaB_6 + 10\ N_2 \rightarrow 20\ BN + 3\ CaO \text{ (T > 1500 °C)}$$

The resulting disordered (amorphous) boron nitride contains 92-95% BN and 5-8% B_2O_3. The remaining B_2O_3 can be evaporated in a second step at temperatures >1500 °C in order to achieve BN concentration >98%. Such annealing also crystallizes BN, the size of the crystallites increasing with the annealing temperature.

h-BN parts can be fabricated inexpensively by hot-pressing with subsequent machining. The parts are made from boron nitride powders adding boron oxide for better compressibility. Thin films of boron nitride can be obtained by chemical vapor deposition from boron trichloride and nitrogen precursors. Combustion of boron powder in nitrogen plasma at 5500 °C yields ultrafine boron nitride used for lubricants and toners.

Boron nitride reacts with iodine fluoride in trichlorofluoromethane at -30 °C to produce an extremely sensitive contact explosive, NI_3, in low yield.

Intercalation of hexagonal BN



Structure of hexagonal boron nitride intercalated with potassium (B_4N_4K)

Similar to graphite, various molecules, such as NH_3 or alkali metals, can be intercalated into hexagonal boron nitride, that is inserted between its layers. Both experiment and theory suggest the intercalation is much more difficult for BN than for graphite.

Preparation of cubic BN

Synthesis of c-BN uses same methods as that of diamond: Cubic boron nitride is produced by treating hexagonal boron nitride at high pressure and temperature, much as synthetic diamond is produced from graphite. Direct conversion of hexagonal boron nitride to the cubic form has been observed at pressures between 5 and 18 GPa and temperatures between 1730 and 3230 °C, that is similar parameters as for direct graphite-diamond conversion. The addition of a small amount of boron oxide can lower the required pressure to 4-7 GPa and temperature to 1500 °C. As in diamond synthesis, to further reduce the conversion pressures and temperatures, a catalyst is added, such as lithium, potassium, or magnesium, their nitrides, their fluoronitrides, water with ammonium compounds, or hydrazine. Other industrial synthesis methods, again

borrowed from diamond growth, use crystal growth in a temperature gradient, or explosive shock wave. The shock wave method is used to produce material called heterodiamond, a superhard compound of boron, carbon, and nitrogen.

Low-pressure deposition of thin films of cubic boron nitride is possible. As in diamond growth, the major problem is to suppress the growth of hexagonal phases (h-BN or graphite, respectively). Whereas in diamond growth this is achieved by adding hydrogen gas, boron trifluoride is used for c-BN. Ion beam deposition, plasma-enhanced chemical vapor deposition, pulsed laser deposition, reactive sputtering, and other physical vapor deposition methods are used as well.

Preparation of wurtzite BN

Wurtzite BN can be obtained via static high-pressure or dynamic shock methods. The limits of its stability are not well defined. Both c-BN and w-BN are formed by compressing h-BN, but formation of w-BN occurs at much lower temperatures close to 1700 °C.

Production statistics

Whereas the production and consumption figures for the raw materials used for BN synthesis, namely boric acid and boron trioxide, are well known, the corresponding numbers for the boron nitride are not listed in statistical reports. An estimate for the 1999 world production is 300 to 350 metric tons. The major producers and consumers of BN are located in the United States, Japan, China and Germany. In 2000, prices varied from about $75/kg to $120/kg for standard industrial-quality h-BN and were about up to $200–$400/kg for high purity BN grades.

Applications

Hexagonal BN

Ceramic BN crucible

Hexagonal BN is the most widely used polymorph. It is a good lubricant at both low and high temperatures (up to 900 °C, even in an oxidizing atmosphere). h-BN lubricant is particularly useful when the electrical conductivity or chemical reactivity of graphite (alternative lubricant) would be problematic. Another advantage of h-BN over graphite is that its lubricity does not require water or gas molecules trapped between the layers. Therefore, h-BN lubricants can be used even in vacuum, e.g. in space applications. The

lubricating properties of fine-grained h-BN are used in cosmetics, paints, dental cements, and pencil leads.

Hexagonal BN was first used in cosmetics around 1940 in Japan. However, because of its high price, h-BN was soon abandoned for this application. Its use was revitalized in the late 1990s with the optimization h-BN production processes, and currently h-BN is used by nearly all leading producers of cosmetic products for foundations, make-up, eye shadows, blushers, kohl pencils, lipsticks and other skincare products.

Because of its excellent thermal and chemical stability, boron nitride ceramics are traditionally used as parts of high-temperature equipment. h-BN can be included in ceramics, alloys, resins, plastics, rubbers, and other materials, giving them self-lubricating properties. Such materials are suitable for construction of e.g. bearings and in steelmaking. Plastics filled with BN have less thermal expansion, higher thermal conductivity and electrical resistivity. Due to its excellent dielectric and thermal properties, BN is used in electronics e.g. as a substrate for semiconductors, microwave-transparent windows, structural material for seals.

Hexagonal BN is used in xerographic process and laser printers as a charge leakage barrier layer of the photo drum. In the automotive industry, h-BN mixed with a binder (boron oxide) is used for sealing oxygen sensors, which provide feedback for adjusting fuel flow. The binder utilizes the unique temperature stability and insulating properties of h-BN.

Parts can be made of h-BN by hot pressing. Union Carbide Corporation produces three grades of BN. HBN, with boron oxide binder, usable to 550-850 °C in oxidizing atmosphere and up to 1600 ° in vacuum, but due to the boron oxide content is sensitive to water. HBR uses calcium borate binder and is usable to 1600 °C. HBC grade uses no binder and can be used to 3000 °C.

Cubic boron nitride

Cubic boron nitride (CBN or c-BN) is widely used as an abrasive. Its usefulness arises from its insolubility in iron, nickel, and related alloys at high temperatures, whereas diamond is soluble in these metals to give carbides. Polycrystalline c-BN (PCBN) abrasives are therefore used for machining steel, whereas diamond abrasives are preferred for aluminum alloys, ceramics, and stone. When in contact with oxygen at high temperatures, BN forms a passivation layer of boron oxide. Boron nitride binds well with metals, due to formation of interlayers of metal borides or nitrides. Materials with cubic boron nitride crystals are often used in the tool bits of cutting tools. For grinding applications, softer binders, e.g. resin, porous ceramics, and soft metals, are used. Ceramic binders can be used as well. Commercial products are known under names "Borazon" (by Diamond Innovations), and "Elbor" or "Cubonite" (by Russian vendors). Similar to diamond, the combination in c-BN of highest thermal conductivity and electrical resistivity is ideal for heat spreaders. Contrary to diamond, large c-BN pellets can be produced in a simple process (called sintering) of annealing c-BN powders in

nitrogen flow at temperatures slightly below the BN decomposition temperature. This ability of c-BN and h-BN powders to fuse allows cheap production of large BN parts.

As cubic boron nitride consists of light atoms and is very robust chemically and mechanically, it is one of the popular materials for X-ray membranes: low mass results in small X-ray absorption, and good mechanical properties allow usage of thin membranes, thus further reducing the absorption.

Amorphous boron nitride

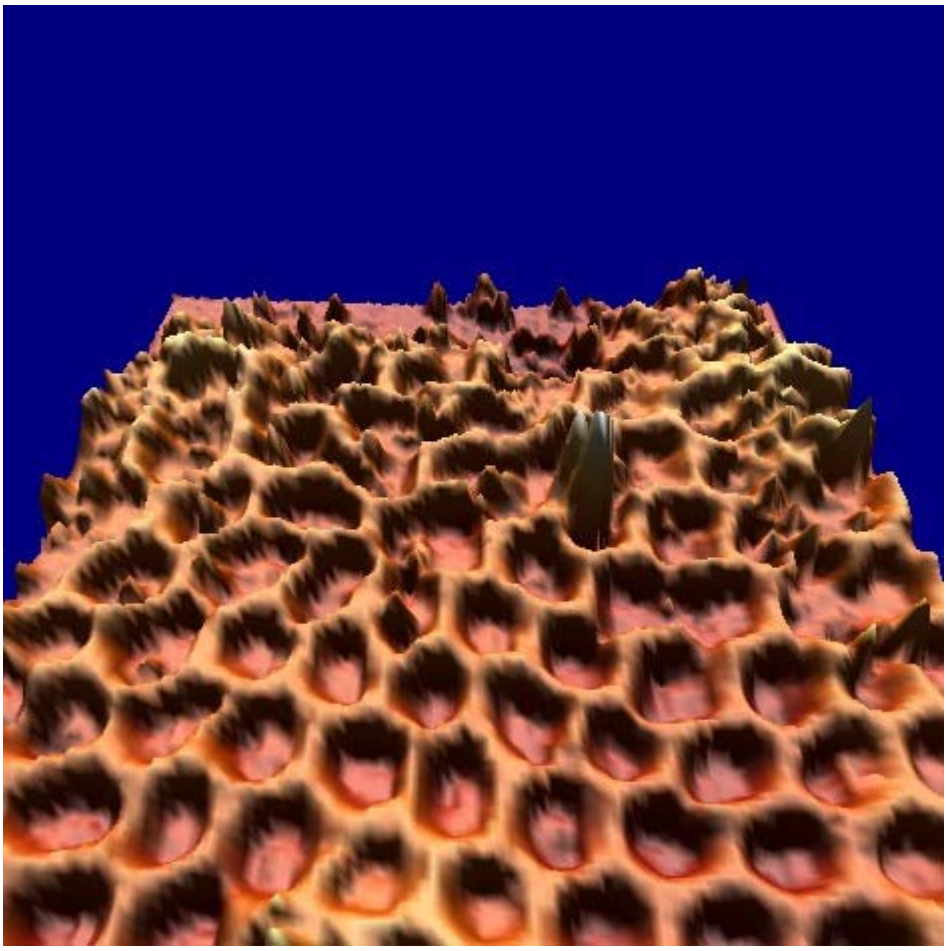
Layers of amorphous boron nitride (a-BN) are used in some semiconductor devices, e.g. MISFETs. They can be prepared by chemical decomposition of trichloroborazine with caesium, or by thermal chemical vapor deposition methods. Thermal CVD can be also used for deposition of h-BN layers, or at high temperatures, c-BN.

Other BN forms

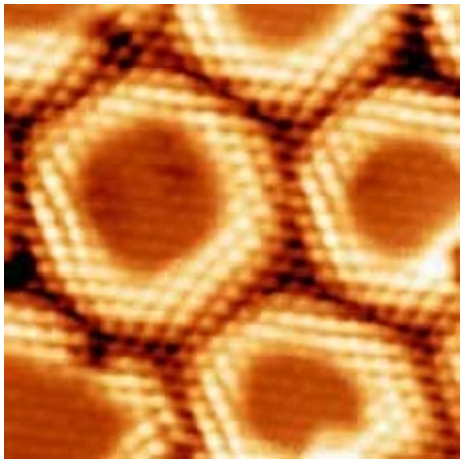
Boron nitride fibers

Hexagonal BN can be prepared in the form of fibers, structurally similar to carbon fibers, by thermal decomposition of extruded borazine ($B_3N_3H_6$) fibers with addition of boron oxide in a nitrogen atmosphere at 1800 °C. An alternative method is thermal decomposition of cellulose fibers impregnated with boric acid or ammonium tetraborate in an atmosphere of ammonia and nitrogen above 1000 °C. Boron nitride fibers are used as reinforcement in composite materials, with the matrix materials ranging from organic resins to ceramics to metals.

Boron nitride nanomesh



Perspective view of nanomesh (structure ends at the back of the figure)



BN nanomesh observed by scanning tunneling microscope. The center of each ring corresponds to the center of the pores

Boron nitride nanomesh is a inorganic nanostructured two-dimensional material. It consists of a single BN layer, which forms by self-assembly a highly regular mesh after high-temperature exposure of a clean rhodium or ruthenium surface to borazine under ultra-high vacuum. The nanomesh looks like an assembly of hexagonal pores. The distance between 2 pore centers is 3.2 nm and the pore diameter is ~2 nm.

The boron nitride nanomesh is not only stable to decomposition under vacuum, air and some liquids, but also up to temperatures of 800 °C. In addition, it shows the extraordinary ability to trap molecules and metallic clusters which have similar sizes to the nanomesh pores, forming a well-ordered array. These characteristics promise interesting applications of the nanomesh in areas like nanocatalysis, surface functionalisation, spintronics, quantum computing and data storage media like hard drives.

Boron nitride nanotubes

Boron nitride nanotubes, were theoretically predicted in 1994 and experimentally discovered in 1995. They can be imagined as a rolled up sheet of boron nitride. Structurally, it is a close analog of the carbon nanotube, namely a long cylinder with diameter of several to hundred nanometers and length of many micrometers, except carbon atoms are alternately substituted by nitrogen and boron atoms. However, the properties of BN nanotubes are very different: whereas carbon nanotubes can be metallic or semiconducting depending on the rolling direction and radius, a BN nanotube is an electrical insulator with a bandgap of ~5.5 eV, basically independent of tube chirality and morphology. In addition, a layered BN structure is much more thermally and chemically stable than a graphitic carbon structure.

All well-established techniques of carbon nanotube growth, such as arc-discharge, laser ablation and chemical vapor deposition, are used to synthesize BN nanotubes. BN nanotubes can also be produced by ball milling of amorphous boron, mixed with a catalyst - iron powder, under NH_3 atmosphere. Subsequent annealing at ~1100 °C in nitrogen flow transforms most of the product into BN.

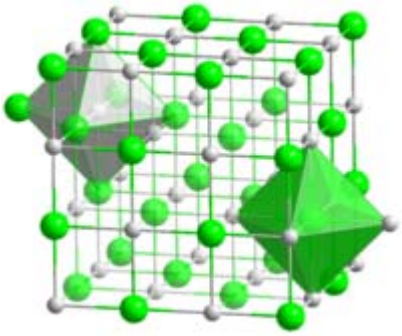
Electrical and field emission properties of the thus prepared nanotubes can be tuned by doping with gold atoms via sputtering of gold on the nanotubes. Doping rare-earth atoms of europium turns a BN nanotube into a phosphor material emitting visible light under electron excitation.

Like BN fibers, boron nitride nanotubes show promise for aerospace applications where integration of boron and in particular the light isotope of boron (^{10}B) into structural materials improves their radiation-shielding properties; the improvement is due to strong neutron absorption by ^{10}B. Such ^{10}BN materials are of particular theoretical value as composite structural materials in future manned interplanetary spacecraft, where absorption-shielding from cosmic ray spallation neutrons is expected to be a particular asset in light construction materials.

Composites containing BN

Addition of boron nitride to silicon nitride ceramics improves the thermal shock resistance of the resulting material. For the same purpose, BN is added also to silicon nitride-alumina and titanium nitride-alumina ceramics. Other materials being reinforced with BN are, e.g., alumina and zirconia, borosilicate glasses, glass ceramics, enamels, and composite ceramics with titanium boride-boron nitride and titanium boride-aluminium nitride-boron nitride and silicon carbide-boron nitride composition.

Cadmium oxide

Cadmium oxide	
	
	
IUPAC name Cadmium oxide Other names Cadmium(II) oxide, Cadmium monoxide	
Identifiers	
CAS number	1306-19-0
ChemSpider	14099
EC number	215-146-2
UN number	2570
RTECS number	EV1925000
SMILES	
InChI	

Properties	
Molecular formula	CdO
Molar mass	128.41 g mol^{-1}
Appearance	colorless powder (alpha form) red-brown crystal (beta form)
Density	8.150 g/cm^3(crystalline), 6.95 g/cm^3 (amorphous) solid.
Melting point	900-1000 °C (decomposition of amorphous form)
Boiling point	1559 °C (sublimation)
Solubility in water	insoluble
Solubility in acid and alkaline	degrades
Electron mobility	531 cm^2/V s
Magnetic susceptibility	-3 × 10^{-5} cm^3/mol
Thermal conductivity	0.7 W/m-K
Structure	
Crystal structure	cubic, cF8
Space group	Fm3m, No. 225
Lattice constant	*a* = 4.6958 Å
Hazards	
MSDS	External MSDS
EU Index	048-002-00-0
EU classification	Carc. Cat. 2 Muta. Cat. 3 Repr. Cat. 3 Very toxic (**T**+) Dangerous for the environment (**N**)
R-phrases	R45, R26, R48/23/25, R62, R63, R68, R50/53
S-phrases	S53, S45, S60, S61
NFPA 704	 0 4 0
Flash point	Non-flammable
Related compounds	
Other anions	Cadmium sulfide Cadmium selenide Cadmium telluride
Other cations	Zinc oxide Mercury oxide

Cadmium oxide is an inorganic compound with the formula CdO. It is one of the main precursors to other cadmium compounds It crystallizes in a cubic rocksalt lattice like sodium chloride, with octahedral cation and anion centers. It occurs naturally as the rare mineral monteponite. Cadmium oxide can be found as a colorless amorphous powder or as brown or red crystals. Cadmium oxide is an n-type semiconductor with a band gap of 2.16 eV at room temperature.

Production and structure

Since cadmium compounds are often found in association with zinc ores, cadmium oxide is a common by-product of zinc refining. It is produced by burning elemental cadmium in air. Pyrolysis of other cadmium compounds, such as the nitrate or the carbonate, also affords this oxide. When pure, it is red but CdO is unusual in being available in many differing colours due to its tendency to form defect structures resulting from anion vacancies. Cadmium oxide is prepared commercially by oxidizing cadmium vapor in air.

Uses

CdO is used as a transparent conductive material, which was prepared as a transparent conducting film back in 1907. Cadmium oxide in the form of thin films has been used in applications such as photodiodes, phototransistors, photovoltaic cells, transparent electrodes, liquid crystal displays, IR detectors, and anti reflection coatings. CdO microparticles undergo bandgap excitation when exposed to UV-A light and is also selective in phenol photodegradation.

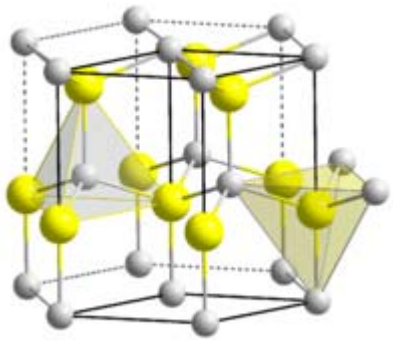
Cadmium oxide is used in cadmium plating baths, electrodes for storage batteries, cadmium salts, catalyst, ceramic glazes, phosphors, and nematocide. Major uses for cadmium oxide is as an ingredient for electroplating baths and in pigments. Most commercial electroplating of cadmium is done by electrodeposition from cyanide baths. These cyanide baths consist of cadmium oxide and sodium cyanide in water, which likely form cadmium cyanide and sodium hydroxide. A typical formula is 32 g/L cadmium oxide and 75 g/L sodium cyanide. The cadmium concentration may vary by as much as 50%. Brighteners are usually added to the bath and the plating is done at room temperature with high purity cadmium anodes.

Reactivity

CdO is a basic oxide and is thus attacked by aqueous acids to give solutions of $[Cd(H_2O)_6]^{2+}$. Upon treatment with strong alkaline solutions, $[Cd(OH)_4]^{2-}$ forms. A thin coat of cadmium oxide forms on the surface of cadmium in moist air at room temperature. Cadmium will oxidize at room temperatures to form CdO. Cadmium vapor and steam will form CdO and hydrogen in a reversible reaction.

Cadmium selenide

Cadmium selenide



IUPAC name
Cadmium selenide

Other names	Cadmium(II) selenide, Cadmoselite
Identifiers	
CAS number	1306-24-7
ChemSpider	14101
SMILES	
InChI	
Properties	
Molecular formula	CdSe
Molar mass	191.37 g/mol
Appearance	Greenish-brown or dark red solid powder
Density	5.816 g/cm^3, solid
Melting point	1268 °C (1541 K)
Solubility in water	Insoluble
Band gap	1.74 eV (direct)
Refractive index (n_D)	2.5
Structure	
Crystal structure	Wurtzite
Space group	C_{6v}^4-$P6_3mc$
Coordination geometry	Tetrahedral
Hazards	
EU Index	048-001-00-5
EU classification	Harmful (**Xn**) Dangerous for the environment (**N**)
R-phrases	R20/21/22, R50/53
S-phrases	(S2), S60, S61
Related compounds	
Other anions	Cadmium oxide, Cadmium sulfide, Cadmium telluride
Other cations	Zinc selenide, Mercury(II) selenide

Cadmium selenide (CdSe) is a solid, binary compound of cadmium and selenium. Common names for this compound are **cadmium(II) selenide**, **cadmium selenide**, and **cadmoselite** (a very rare mineral).

Cadmium selenide is a semiconducting material, but has yet to find many applications in manufacturing. This material is transparent to infra-red (IR) light, and has seen limited use in windows for instruments utilizing IR light.

Much current research on cadmium selenide has focused on nanoparticles. Researchers are concentrating on developing controlled syntheses of CdSe nanoparticles. In addition to synthesis, scientists are working to understand the properties of cadmium selenide, as well as apply these materials in useful ways.

Structure

Three crystalline forms of CdSe are known: wurtzite (hexagonal), sphalerite (cubic) and rock-salt (cubic). The sphalerite CdSe structure is unstable and converts to the wurtzite form upon moderate heating. The transition starts at about 130 °C, and at 700 °C it completes within a day. The rock-salt structure is only observed under high pressure.

Production

The production of cadmium selenide has been carried out in two different ways. The preparation of bulk crystalline CdSe is done by the High-Pressure Vertical Bridgman method or High-Pressure Vertical Zone Melting.

Cadmium selenide may also be produced in the form of nanoparticles. Several methods for the production of CdSe nanoparticles have been developed: arrested precipitation in solution, synthesis in structured media, high temperature pyrolysis, sonochemical, and radiolytic methods are just a few.

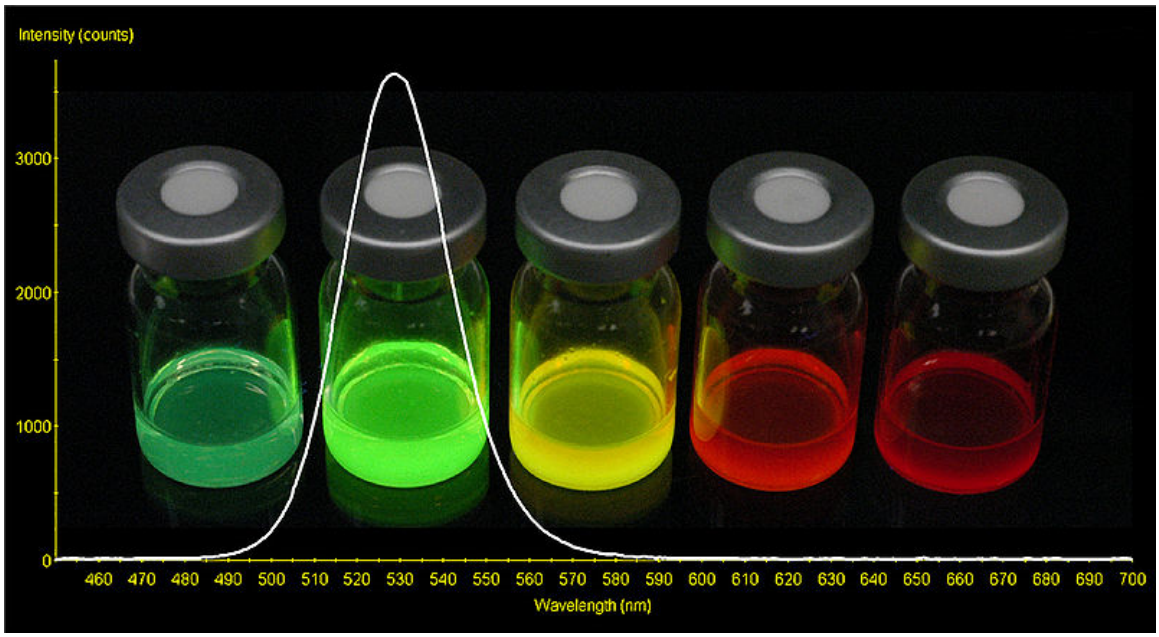
Production of cadmium selenide by arrested precipitation in solution is performed by introducing alkylcadmium and trioctylphosphine selenide (TOPSe) precursors into a heated solvent under controlled conditions.

$$Me_2Cd + TOPSe \rightarrow CdSe + (byproducts).$$

Synthesis in structured environments refers to the production of cadmium selenide in liquid crystal or surfactant solutions. The addition of surfactants to solutions often results in a phase change in the solution leading to a liquid crystallinity. A liquid crystal is similar to a solid crystal in that the solution has long range translational order. Examples of this ordering are layered alternating sheets of solution and surfactant, micelles, or even a hexagonal arrangement of rods.

High temperature pyrolysis synthesis is usually carried out using an aerosol containing a mixture of volatile cadmium and selenium precursors. The precursor aerosol is then carried through a furnace with an inert gas, such as hydrogen, nitrogen, or argon. In the furnace the precursors react to form CdSe as well as several by-products.

Applications



A photograph and representative spectrum of photoluminescence from colloidal CdSe quantum dots excited by UV light.

Cadmium selenide in its wurtzite crystal structure is an important II-VI semiconductor. As a semiconductor CdSe is an n-type semiconductor, which is difficult to dope p-type, however p-type doping has been achieved using nitrogen. CdSe is also being developed for use in opto-electronic devices, laser diodes, nanosensing, and biomedical imaging. They are also used being tested for use in high-efficiency solar cells

Most of the usefulness of CdSe stems from nanoparticles, that is particles with sizes below 100 nm. CdSe particles of this size exhibit a property known as quantum confinement. Quantum confinement results when the electrons in a material are confined to a very small volume. Quantum confinement is size dependent, meaning the properties of CdSe nanoparticles are tunable based on their size.

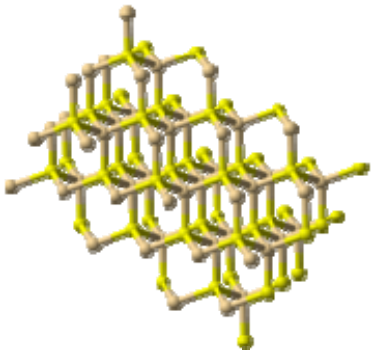
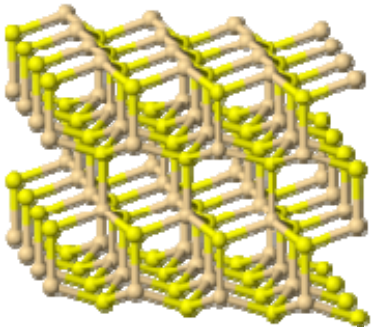
Since CdSe nanoparticles have a size dependent fluorescence spectrum, they are finding applications in optical devices such as laser diodes. Using these particles, engineers are able to manufacture laser diodes that cover a large part of the electromagnetic spectrum.

Along similar lines, doctors are developing these materials for use in biomedical imaging applications. Human tissue is permeable to far infra-red light. By injecting appropriately prepared CdSe nanoparticles into injured tissue, it may be possible to image the tissue in those injured areas.

Safety information

Cadmium is a toxic heavy metal and appropriate precautions should be taken when handling it and its compounds. Selenides are toxic in large amounts. .

Cadmium sulfide

Cadmium sulfide	
	
	
Other names Cadmium(II) sulfide, Greenockite Hawleyite	
Identifiers	
CAS number	1306-23-6 ✓
ChemSpider	7969586 ✓
UNII	057EZR4Z7Q ✓
EC number	215-147-8
UN number	2570
RTECS number	EV3150000
SMILES	
InChI	

Properties	
Molecular formula	CdS
Molar mass	144.46 g/mol
Appearance	Yellow-orange solid.
Density	4.82 g/cm^3, solid.
Melting point	1750 °C at 100 bar (10 MPa)
Boiling point	980 °C *subl.*
Solubility in water	insoluble
Refractive index (n_D)	2.51
Structure	
Crystal structure	Hexagonal, Cubic
Hazards	
MSDS	ICSC 0404
EU Index	048-010-00-4
EU classification	Carc. Cat. 2 Muta. Cat. 3 Repr. Cat. 3 Toxic (**T**) Dangerous for the environment (**N**)
R-phrases	R45, R22, R48/23/25, R62, R63, R68, R50/53
S-phrases	S53, S45, S61
NFPA 704	 0 3 0
Flash point	Non-flammable
Related compounds	
Other anions	Cadmium oxide Cadmium selenide
Other cations	Zinc sulfide Mercury sulfide

Cadmium sulfide is the inorganic compound with the formula CdS. Cadmium sulfide is yellow solid. It occurs in nature with two different crystal structures as the rare minerals greenockite and hawleyite, but is more prevalent as an impurity substituent in the similarly structured zinc ores sphalerite and wurtzite, which are the major economic sources of cadmium. As a compound that is easy to isolate and purify, it is the principal source of cadmium for all commercial applications.

Production

Cadmium sulfide can be prepared by the precipitation from soluble cadmium(II) salts with sulfide ion and this has been used in the past for gravimetric analysis and qualitative inorganic analysis.

Pigment production usually involves the precipitation of CdS, the washing of the precipitate to remove soluble cadmium salts followed by calcination (roasting) to convert it to the hexagonal form followed by milling to produce a powder. When cadmium sulfide selenides are required the CdSe is co-precipitated with CdS and the cadmium sulfoselenide is created during the calcination step.

Industrially the production of thin films of CdS, required in e.g. photoresistors and chemical bath deposition (CBD), has been investigated using the hydrolysis of thiourea as the source of sulfide anions and an ammonium salt /ammonia buffer solution to control pH:

$$Cd^{2+} + 4\ NH_3 \rightarrow [Cd(NH_3)_4]^{2+}$$
$$(NH_2)_2CS + OH^- \rightarrow SH^- + H_2O + H_2CN_2$$
$$SH^- + Cd^{2+} \rightarrow CdS + H^+$$

Cadmium sulfide can be produced from volatile cadmium alkyls, an example is the reaction of dimethylcadmium with diethyl sulfide to produce a film of CdS using metalorganic vapour phase epitaxy techniques.

The preparative route and the subsequent treatment of the product, affects the polymorphic form that is produced. It has been asserted that chemical precipitation methods result in the cubic zincblende form

Routes to thin films of CdS

Thin films of CdS are components in some photoresistors and solar cells. Various methods have been used to deposit these thin films, for example (note: there is a large body of research in this area and only representative references are given):

- Chemical bath deposition, CBD
- Sol gel techniques
- MOCVD
- Sputtering
- Electrochemical deposition
- Spraying with precursor cadmium salt, sulfur compound and dopant
- Screen printing using a slurry containing dispersed CdS

Reactions

Cadmium sulfide is soluble in (actually degraded by) acids, and this conversion has been investigated as a method of extracting the pigment from waste polymers e.g. HDPE pipes:

$$CdS + 2\ HCl \rightarrow CdCl_2 + H_2S$$

When sulfide solutions containing dispersed CdS particles are irradiated with light hydrogen gas is generated:

$$H_2S \rightarrow H_2 + S\ \Delta H_f = +9.4\ \text{kcal/mol}$$

The proposed mechanism involves the electron/hole pairs created when incident light is absorbed by the cadmium sulfide followed by these reacting with water and sulfide:

Production of an electron hole pair
$CdS + h\nu \rightarrow e^- + hole^+$
Reaction of electron
$2e^- + 2H_2O \rightarrow H_2 + 2OH^-$
Reaction of hole
$2hole^+ + S^{2-} \rightarrow S$

Structure and physical properties

Cadmium sulfide has, like zinc sulfide, two crystal forms; the more stable hexagonal wurtzite structure (found in the mineral Greenockite) and the cubic zinc blende structure (found in the mineral Hawleyite). In both of these forms the cadmium and sulfur atoms are four coordinate. There is also a high pressure form with the NaCl rock salt structure.

Cadmium sulfide is a direct band gap semiconductor (gap 2.42 eV). The magnitude of its band gap means that it appears coloured.
As well as this obvious property others properties result:

- the conductivity increases when irradiated with light (leading to uses as a photoresistor)
- when combined with a p-type semiconductor it forms the core component of a photovoltaic (solar) cell and a CdS/Cu_2S solar cell was one of the first efficient cells to be reported (1954)
- when doped with for example Cu^+ ("activator") and Al^{3+} ("coactivator") CdS luminesces under electron beam excitation (cathodoluminescence) and is used as phosphor
- both polymorphs are piezoelectric and the hexagonal is also pyroelectric
- electroluminescence
- CdS crystal can act as a solid state laser

Applications

CdS is mainly used as a pigment.

CdS and cadmium selenide are used in manufacturing of photoresistors (light dependent resistors) sensitive to visible and near infrared light.

Pigment

CdS is known as cadmium yellow (CI pigment yellow 37). By adding varying amounts of selenium as selenide it is possible to obtain a range of colors for example CI pigment orange 20 and CI pigment red 108.
Synthetic cadmium pigments based on cadmium sulfide are valued for their good thermal stability, light and weather fastness, chemical resistance and high opacity. The general commercial availability of cadmium sulfide from the 1840s lead to its adoption by artists notably Van Gogh, Monet (in his London series and other works) and Matisse (*Bathers by a river* 1916-1919). The presence of cadmium in paints has been used to detect forgeries in paintings alleged to have been produced prior to the 19th century. CdS is used as pigment in plastics.